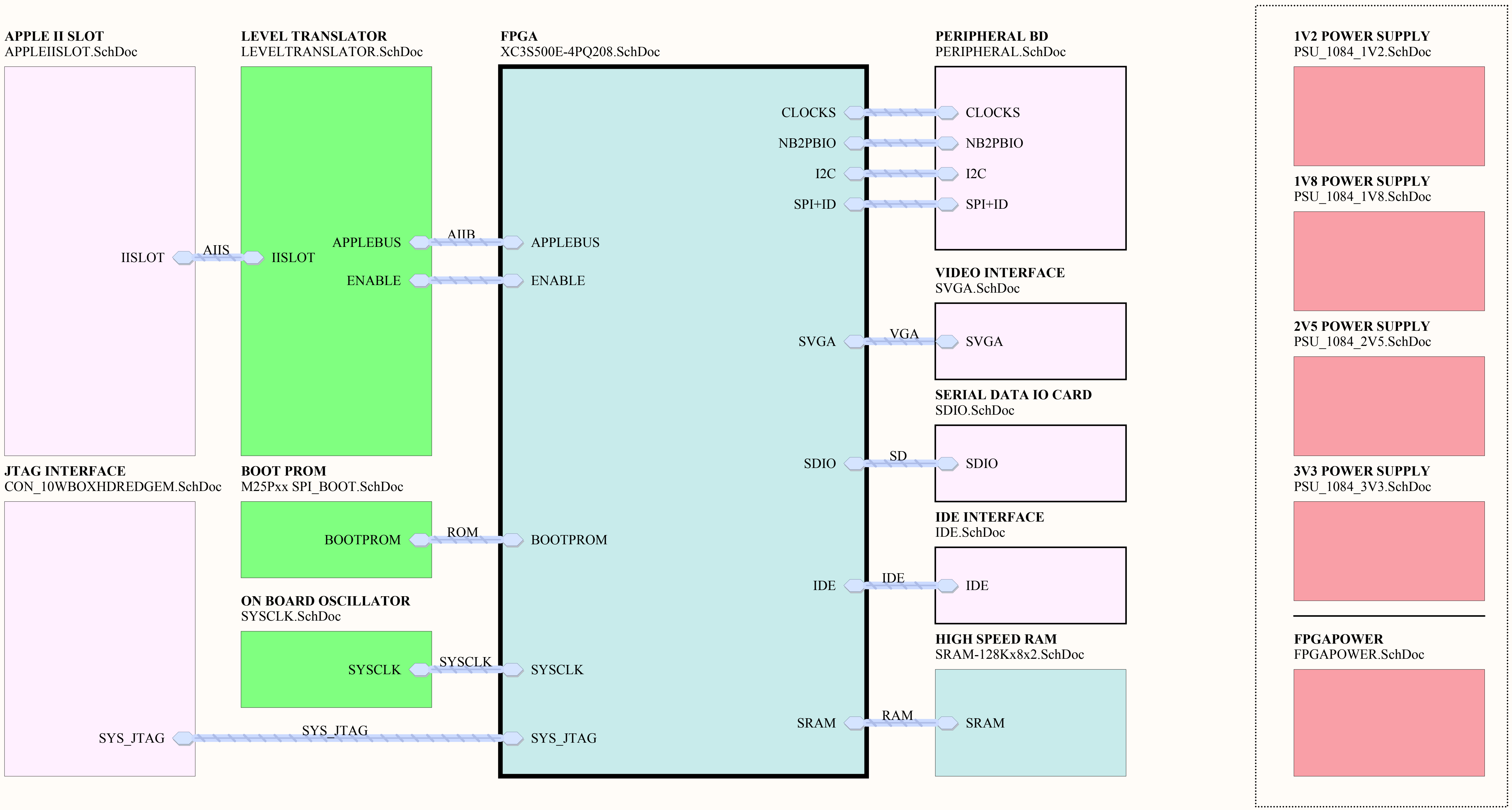
NOTES IN TURQUOISE REFER TO XILINX DOCUMENTATION.



TOP LEVEL COLOUR CODE:

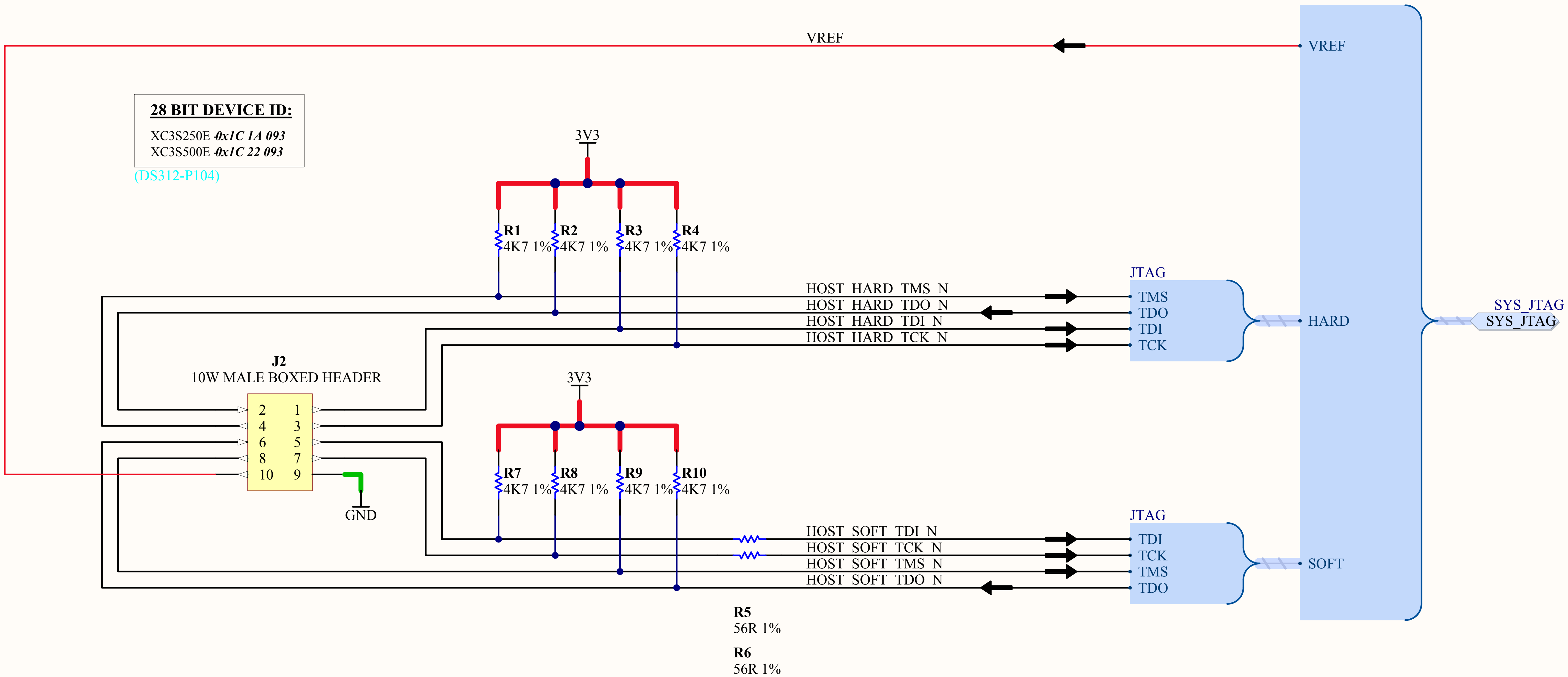
PINK: I/O CONNECTION/REAL WORLD ACCESS
GREEN: INTERNAL PROCESS/SERVICE
BLUE: SYSTEM CORE/USER AVAILABLE
RED: POWER RELATED SERVICE

FD2
Fiducial - Round

FD1
Fiducial - Round

SN1
BARCODE/SERIAL NUMBER
SERIAL NUMBER

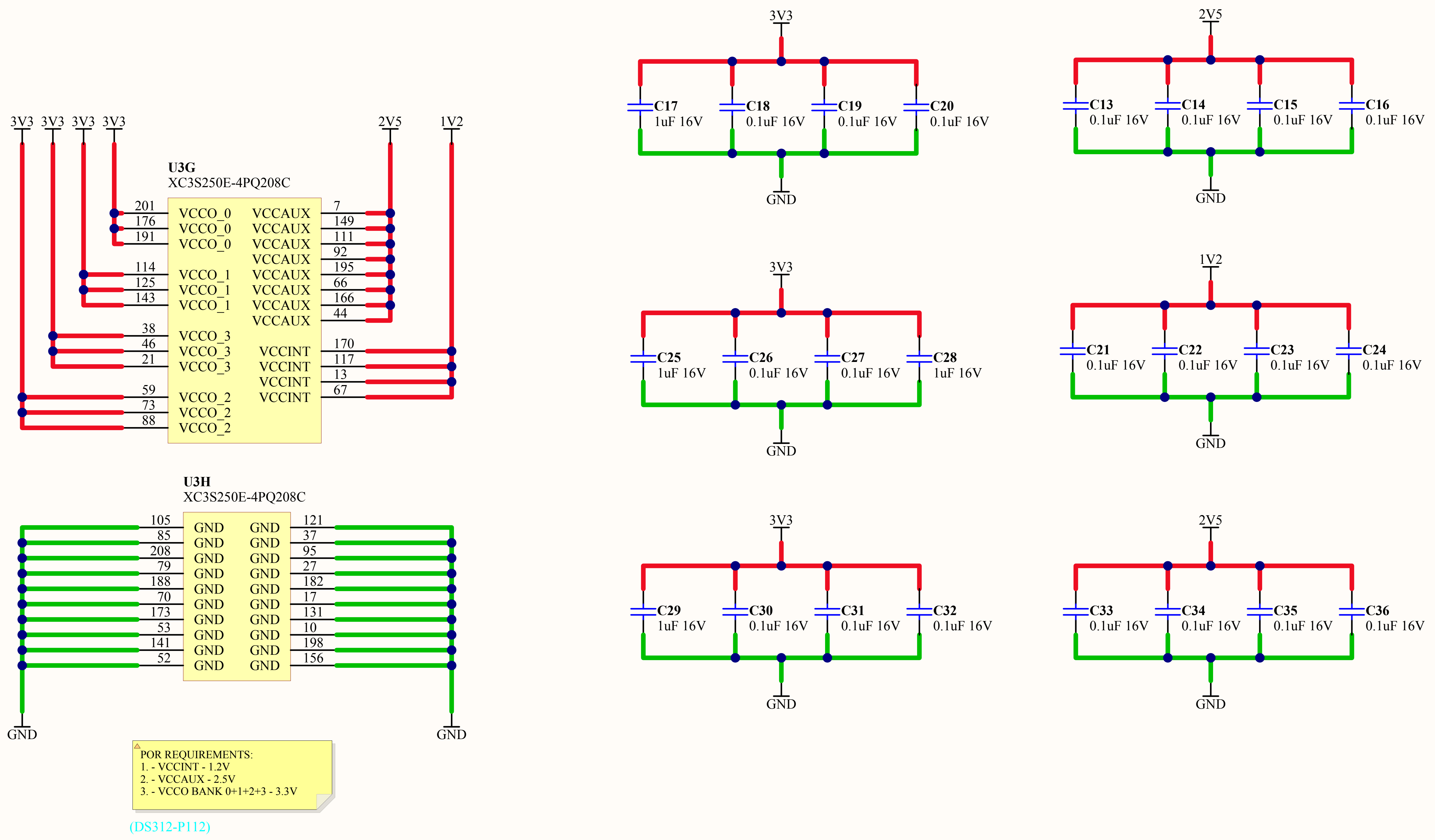
TITLE: Carte Blanche for the Apple II	www.AppleLogic.org Carte Blanche Apple II FPGA Peripheral Board
SIZE: A4 VERSION: CB500E CHKD: SRKH	
DATE: 30/09/2009 TIME: 9:39:02 PM SHEET 1 OF 18	
FILE: C:\AppleLogic\CarteBlanche\CB1_TEMPLATE\CarteBlanche.SchDoc	



JTAG PROGRAMMING INTERFACE

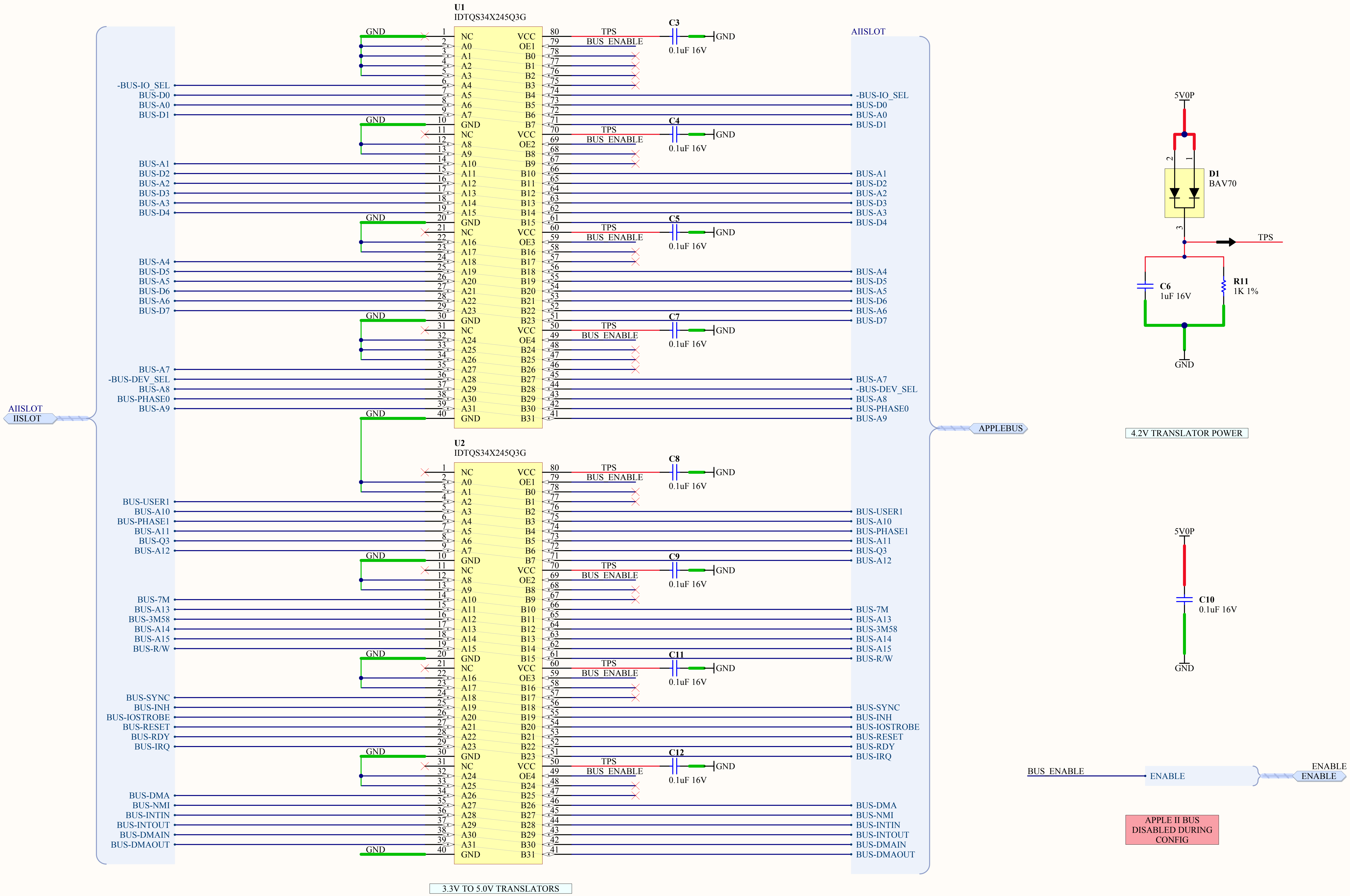
IF YOU ARE CONNECTING THIS INTERFACE TO
USER BOARD A OR USER BOARD B
DO NOT CONNECT THE REF PIN. REFER
TO THE APPLELOGIC WEBSITE FOR DETAILS

TITLE: **JTAG INTERFACE**		www.AppleLogic.org Carte Blanche Apple II FPGA Peripheral Board
SIZE: A4	VERSION: CB500E	CHKD: SRKH
DATE: 30/09/2009	TIME: 9:39:02 PM	SHEET 2 OF 18
FILE: C:\AppleLogic\CarteBlanche\CB1_TEMPLATE\CON_10WBOXHDREDGEM.SchDoc		



TITLE: FPGA POWER CONFIG.		
SIZE: A4	VERSION: CB500E	CHKD: SRKH
DATE: 30/09/2009	TIME: 9:39:02 PM	SHEET 3 OF 18
FILE: C:\AppleLogic\CarteBlanche\CB1_TEMPLATE\FPGAPOWER.SchDoc		

www.AppleLogic.org
Carte Blanche
Apple II FPGA Peripheral Board



TITLE: **AII BUS LEVEL TRANSLATORS**

www.AppleLogic.org

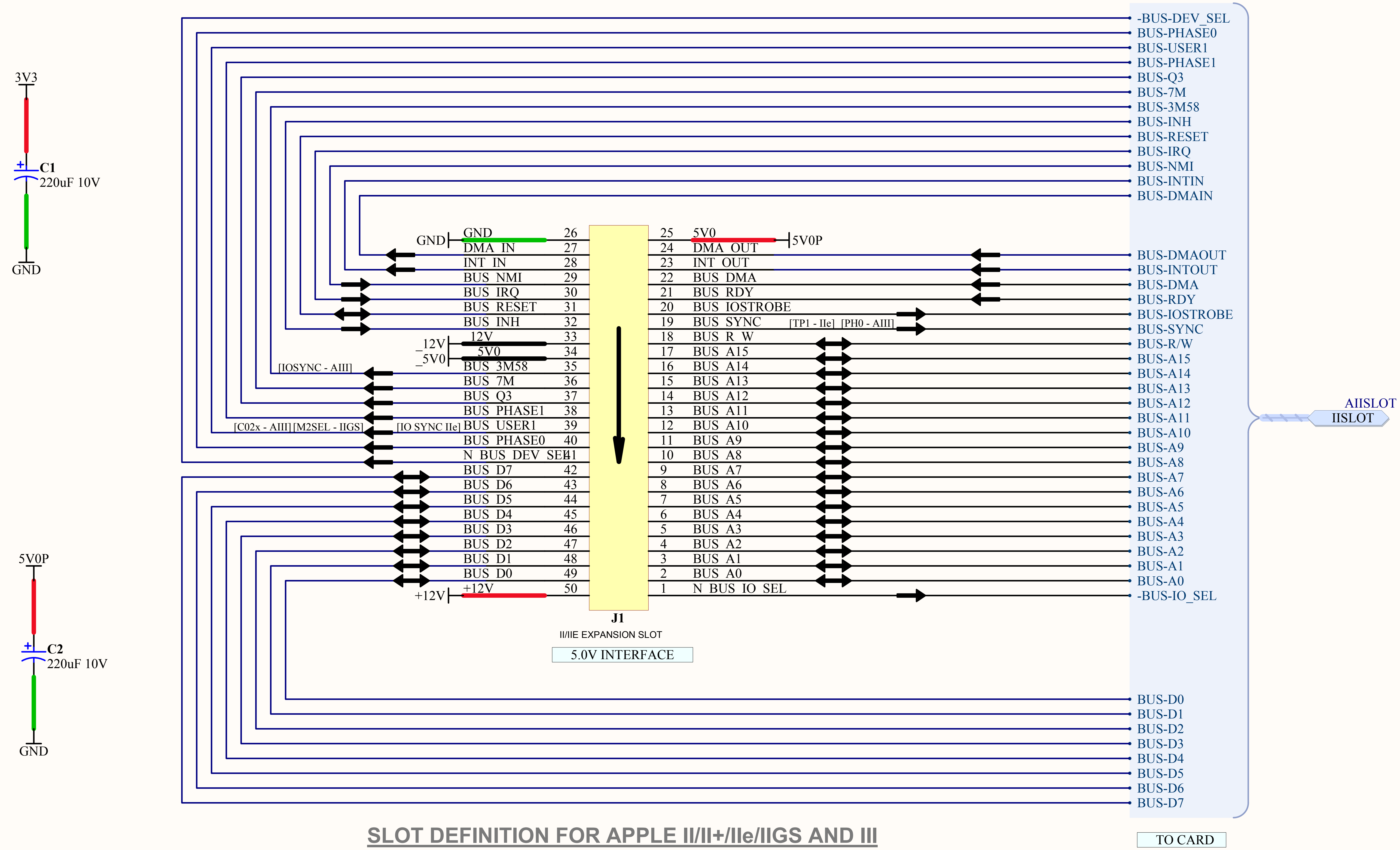
Carte Blanche

Apple II FPGA Peripheral Board

SIZE: A3 | VERSION: CB500E | CHKD: SRKH

DATE: 30/09/2009 | TIME: 9:39:02 PM | SHEET 4 OF 18

FILE: C:\AppleLogic\CarteBlanche\CB1_TEMPLATE\LEVELTRANSLATOR.SchDoc



SLOT DEFINITION FOR APPLE II/II+/IIe/IIGS AND III

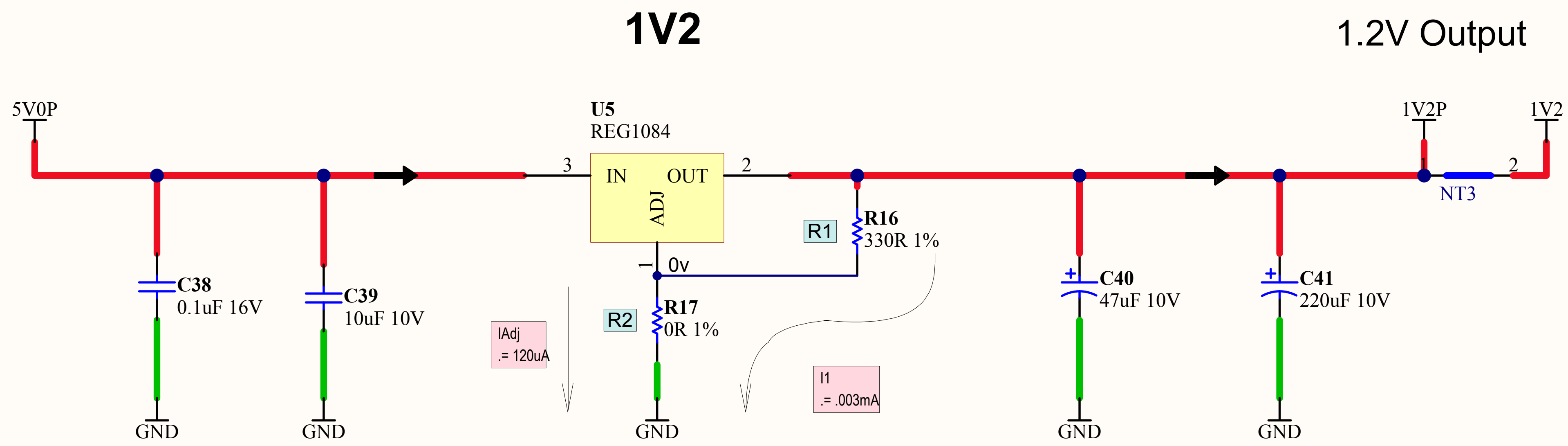
TO CARD

TITLE: **APPLE II BUS INTERFACE**		
SIZE: **A4**	VERSION: **CB500E**	CHKD: **SRKH**
DATE: 30/09/2009	TIME: 9:39:03 PM	SHEET 5 OF 18
FILE: C:\AppleLogic\CarteBlanche\CB1_TEMPLATE\APPLEIISLOT.SchDoc		

www.AppleLogic.org

Carte Blanche

Apple II FPGA Peripheral Board



R1 TO BE IN THE 100R RANGE

Vout = 1.25 $\left(1+\frac{R2}{R1}\right)$ + [(IAdj) (R2)]

IAdj = 120uA

Vout = 1.25 $\left(1+\frac{0}{330}\right)$ + [0.000,120 x 120]

Vout = (1.25 x 1.00) + 0.0144

Vout = 1.25 + 0.0144

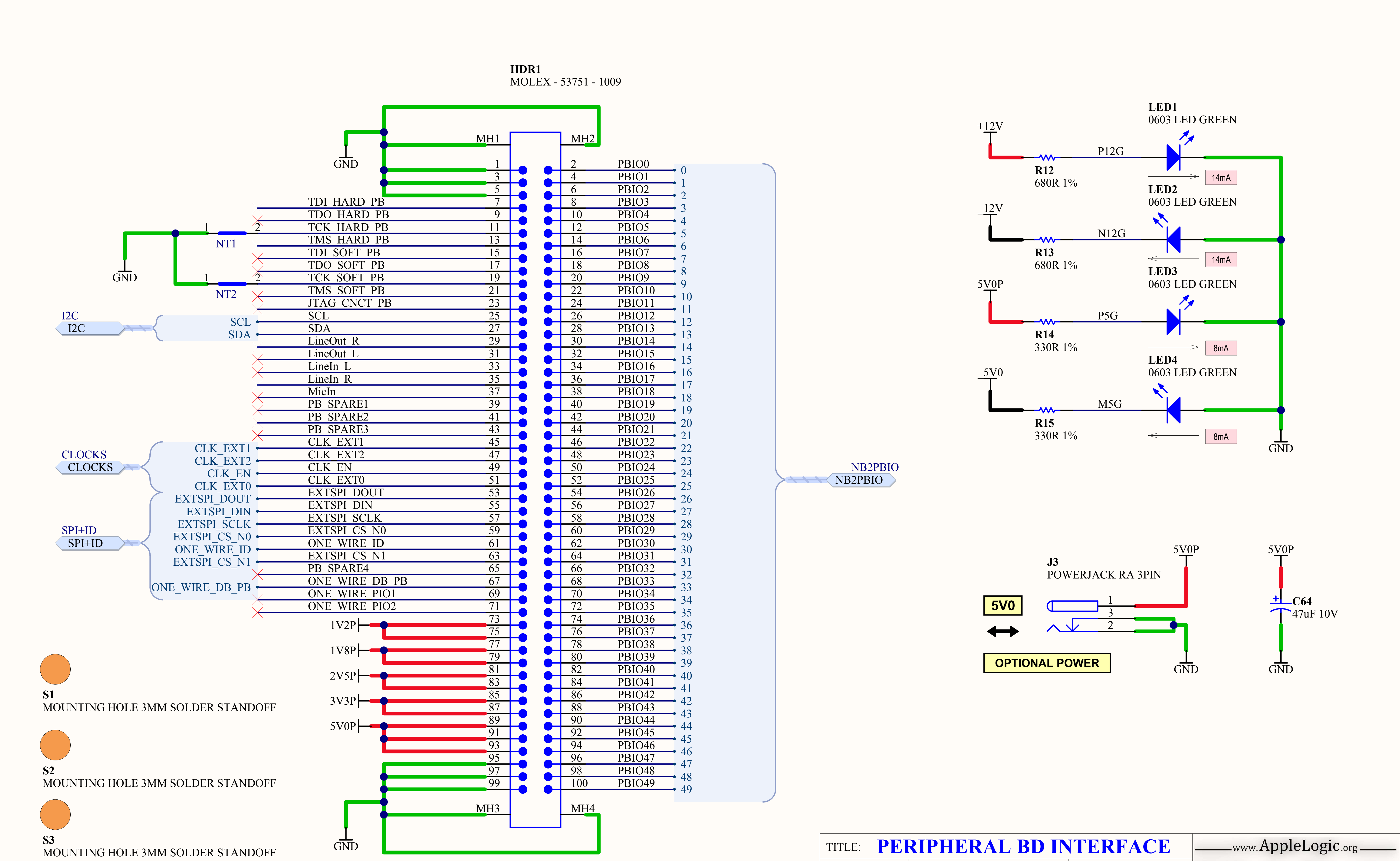
Vout = 1.2644v

TITLE: **1V2 POWER SUPPLY**		
SIZE: **A4**	VERSION: **CB500E**	CHKD: **SRKH**
DATE: 30/09/2009	TIME: 9:39:03 PM	SHEET 6 OF 18
FILE: *C:\AppleLogic\CarteBlanche\CB1_TEMPLATE\PSU_1084_1V2.SchDoc*		

www.AppleLogic.org

Carte Blanche

Apple II FPGA Peripheral Board



TITLE: **PERIPHERAL BD INTERFACE**

SIZE: A4 | VERSION: CB500E | CHKD: SRKH

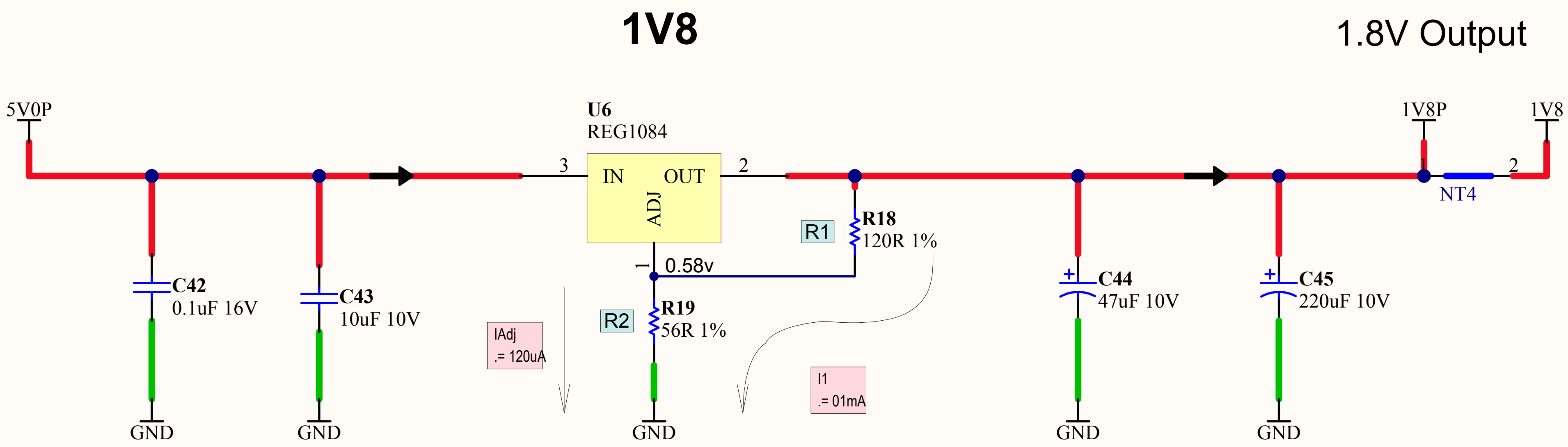
DATE: 30/09/2009 | TIME: 9:39:03 PM | SHEET 7 OF 18

FILE: C:\AppleLogic\CarteBlanche\CB1_TEMPLATE\PERIPHERAL.SchDoc

www.AppleLogic.org

Carte Blanche

Apple II FPGA Peripheral Board



R1 TO BE IN THE 100R RANGE

Vout = $1.25\,(1+\frac{R2}{R1}) + [(IAdj)\,(R2)]$

IAdj = 120uA

Vout = $1.25\,(1+\frac{56}{120}) + [0.000,120 \times 120]$

Vout = (1.25 x 1.455) + 0.0144

Vout = 1.818 + 0.0144

Vout = 1.8324v

TITLE: **1V8 POWER SUPPLY**		
SIZE: **A4**	VERSION: **CB500E**	CHKD: **SRKH**
DATE: 30/09/2009	TIME: 9:39:03 PM	SHEET 8 OF 18
FILE: *C:\AppleLogic\CarteBlanche\CB1_TEMPLATE\PSU_1084_1V8.SchDoc*		

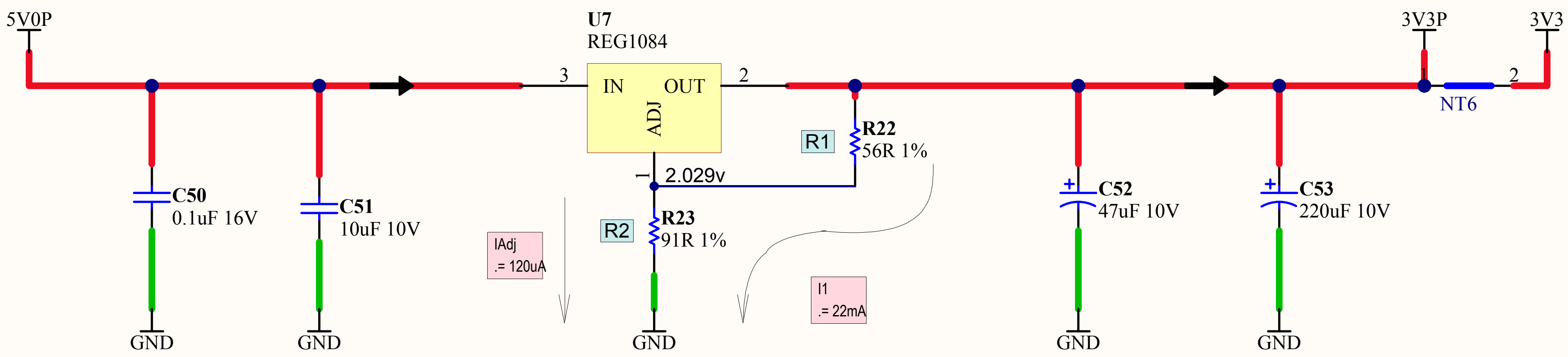
www.AppleLogic.org

Carte Blanche

Apple II FPGA Peripheral Board

3V3

3.3V Output



R1 TO BE IN THE 100R RANGE

$V_{out} = 1.25\,(1+\frac{R2}{R1}) + [(IAdj)\,(R2)]$

IAdj = 120uA

$V_{out} = 1.25\,(1+\frac{91}{56}) + [0.000{,}120 \times 91]$

$V_{out} = (1.25 \times 2.625) + 0.01092$

$V_{out} = 3.28125 + 0.01092$

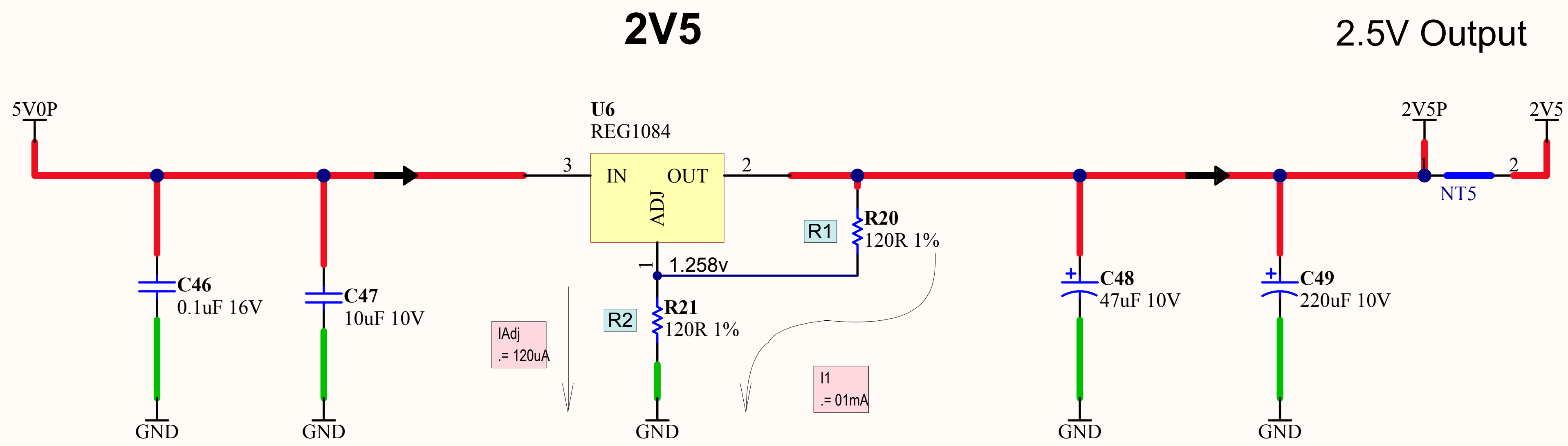
Vout = 3.292v

TITLE: **3V3 POWER SUPPLY**		
SIZE: **A4**	VERSION: **CB500E**	CHKD: **SRKH**
DATE: 30/09/2009	TIME: 9:39:03 PM	SHEET 9 OF 18
FILE: *C:\AppleLogic\CarteBlanche\CB1_TEMPLATE\PSU_1084_3V3.SchDoc*		

www.AppleLogic.org

Carte Blanche

Apple II FPGA Peripheral Board



R1 TO BE IN THE 100R RANGE

Vout = 1.25 $(1+\frac{R2}{R1})$ + [(IAdj) (R2)]

IAdj = 120uA

Vout = 1.25 $(1+\frac{120}{120})$ + [0.000,120 x 120]

Vout = (1.25 x 2.00) + 0.0144

Vout = 2.500 + 0.0144

Vout = 2.5144v

TITLE: **2V5 POWER SUPPLY**

SIZE: **A4** VERSION: **CB500E** CHKD: **SRKH**

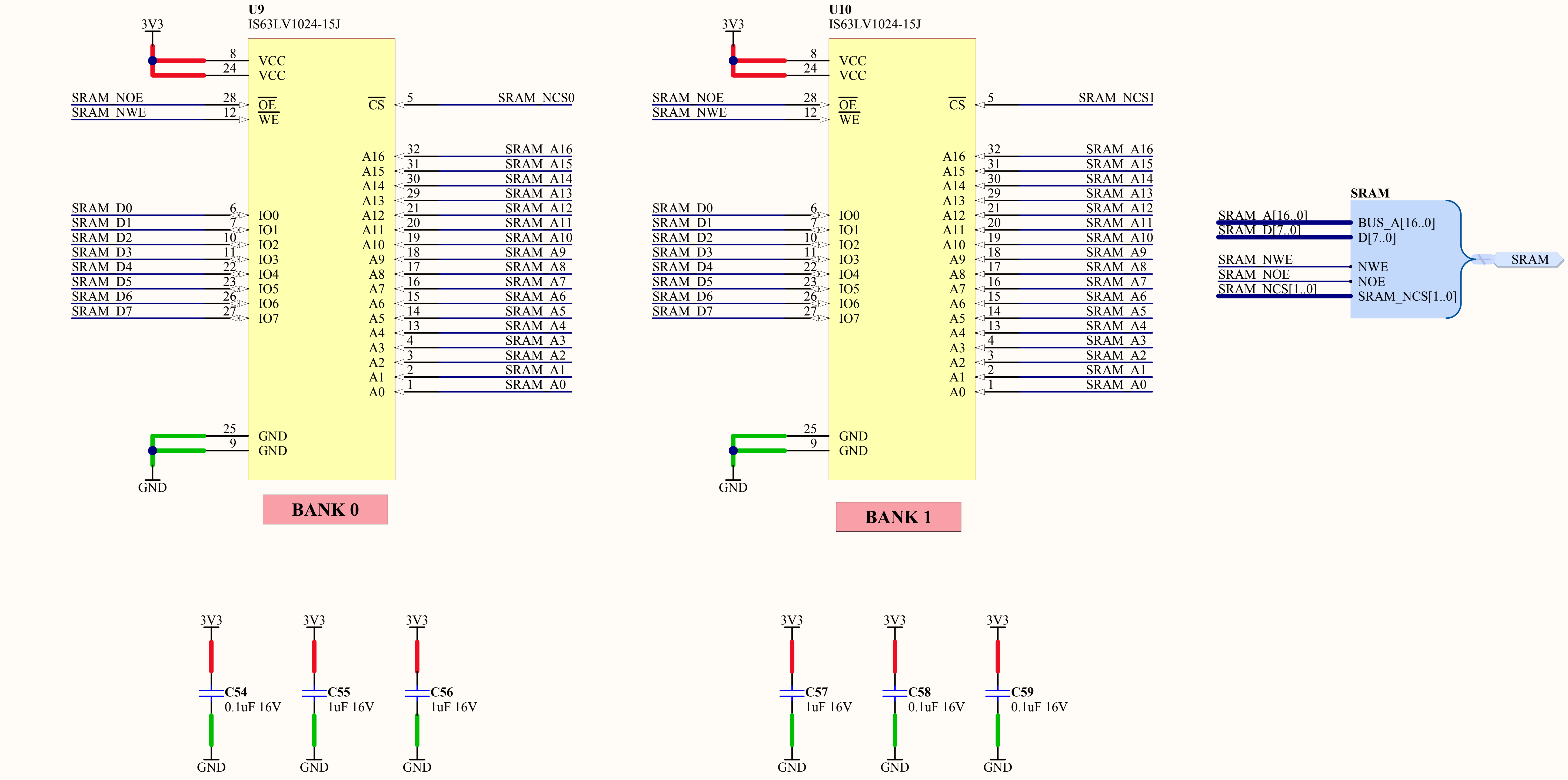
DATE: 30/09/2009 TIME: 9:39:03 PM SHEET 10 OF 18

FILE: *C:\AppleLogic\CarteBlanche\CB1_TEMPLATE\PSU_1084_2V5.SchDoc*

www.AppleLogic.org

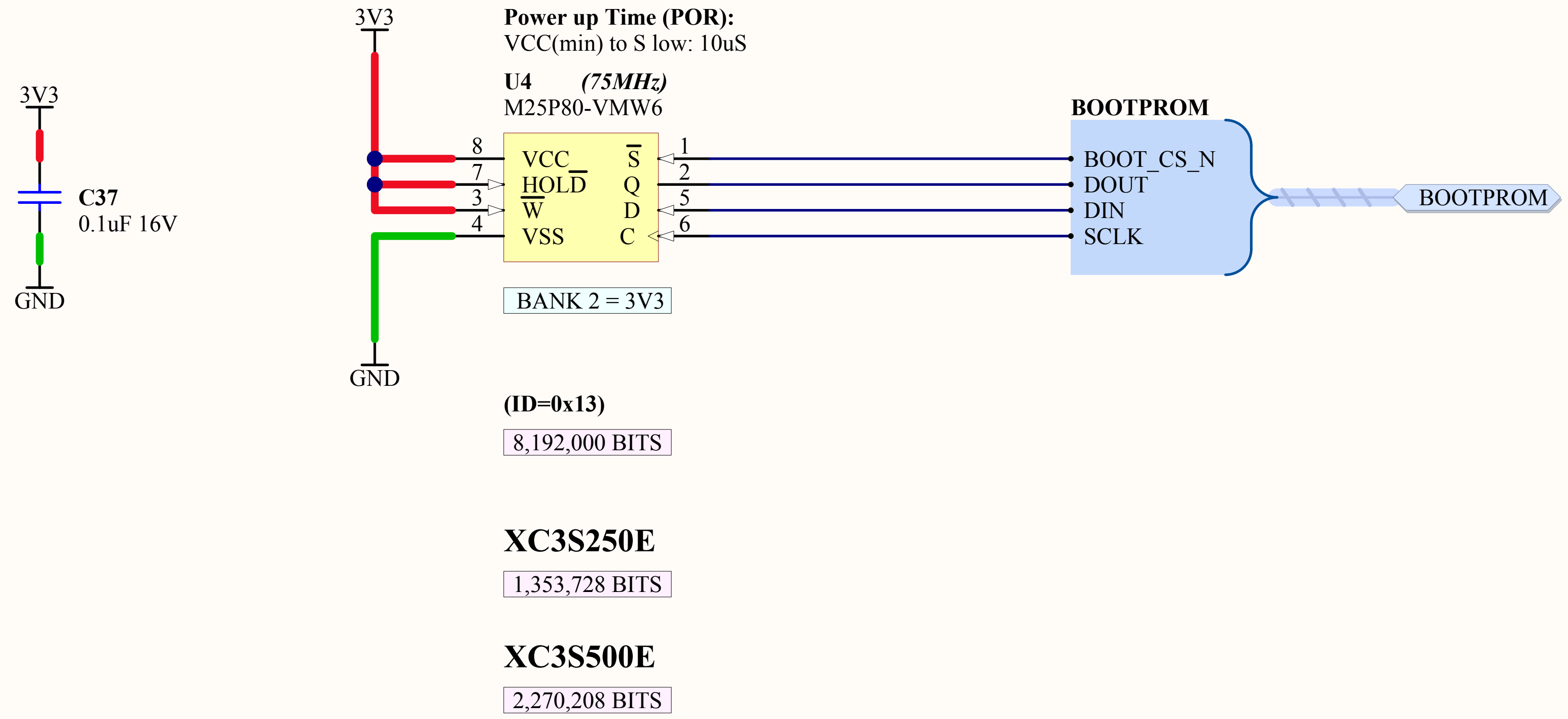
Carte Blanche

Apple II FPGA Peripheral Board

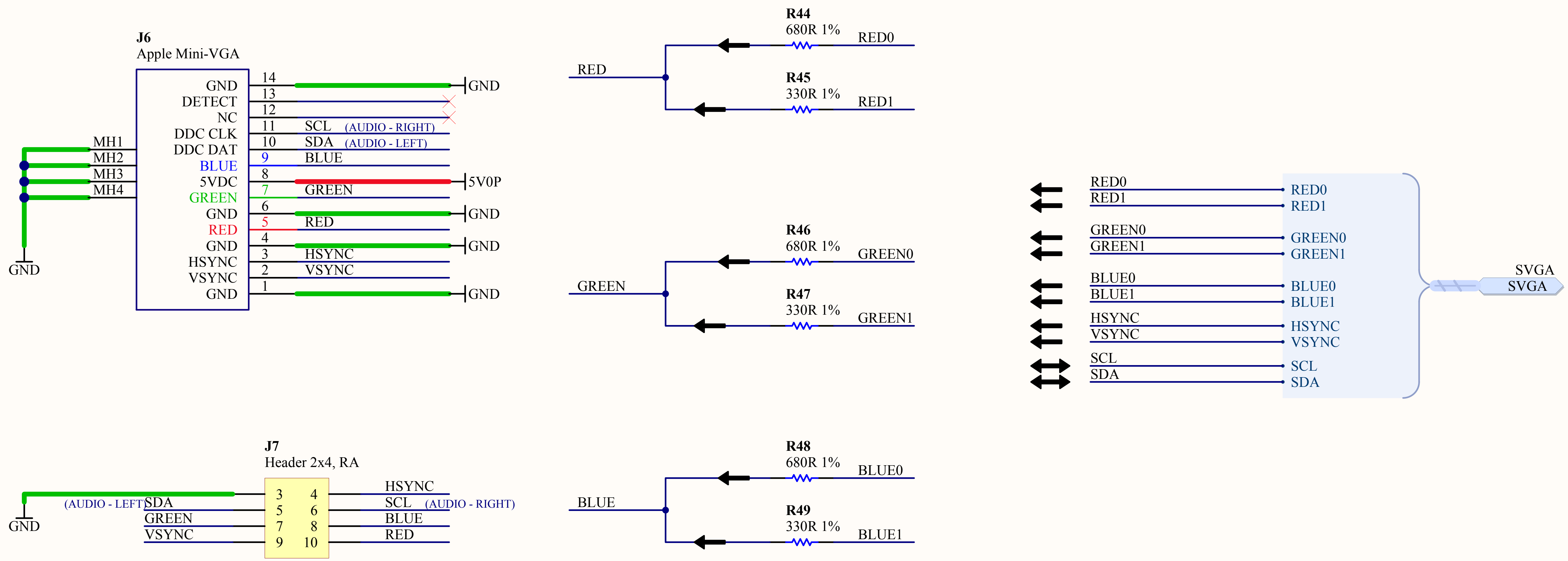


TITLE: 256K x8 SRAM MEMORY	
SIZE: A4	VERSION: CB500E	CHKD: SRKH
DATE: 30/09/2009	TIME: 9:39:03 PM	SHEET 11 OF 18
FILE: C:\AppleLogic\CarteBlanche\CB1_TEMPLATE\SRAM-128Kx8x2.SchDoc		

www.AppleLogic.org
Carte Blanche
Apple II FPGA Peripheral Board



TITLE: SPI SYSTEM BOOT FLASH			www.AppleLogic.org Carte Blanche Apple II FPGA Peripheral Board
SIZE: A4	VERSION: CB500E	CHKD: SRKH	
DATE: 30/09/2009	TIME: 9:39:03 PM	SHEET 12 OF 18	
FILE: C:\AppleLogic\CarteBlanche\CB1_TEMPLATE\M25Pxx SPI_BOOT.SchDoc			

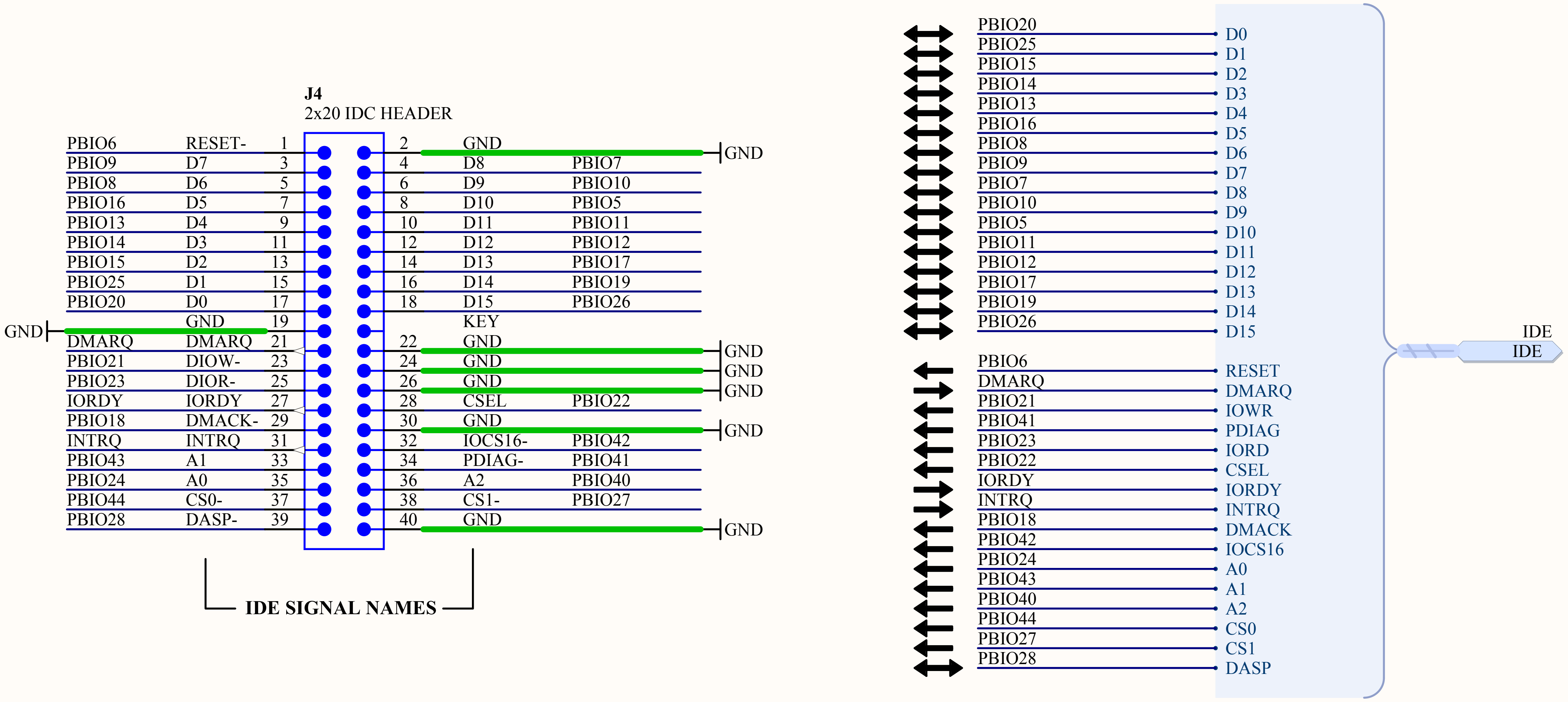


SVGA DB15 CONNECTOR
SVGAIO.SchDoc

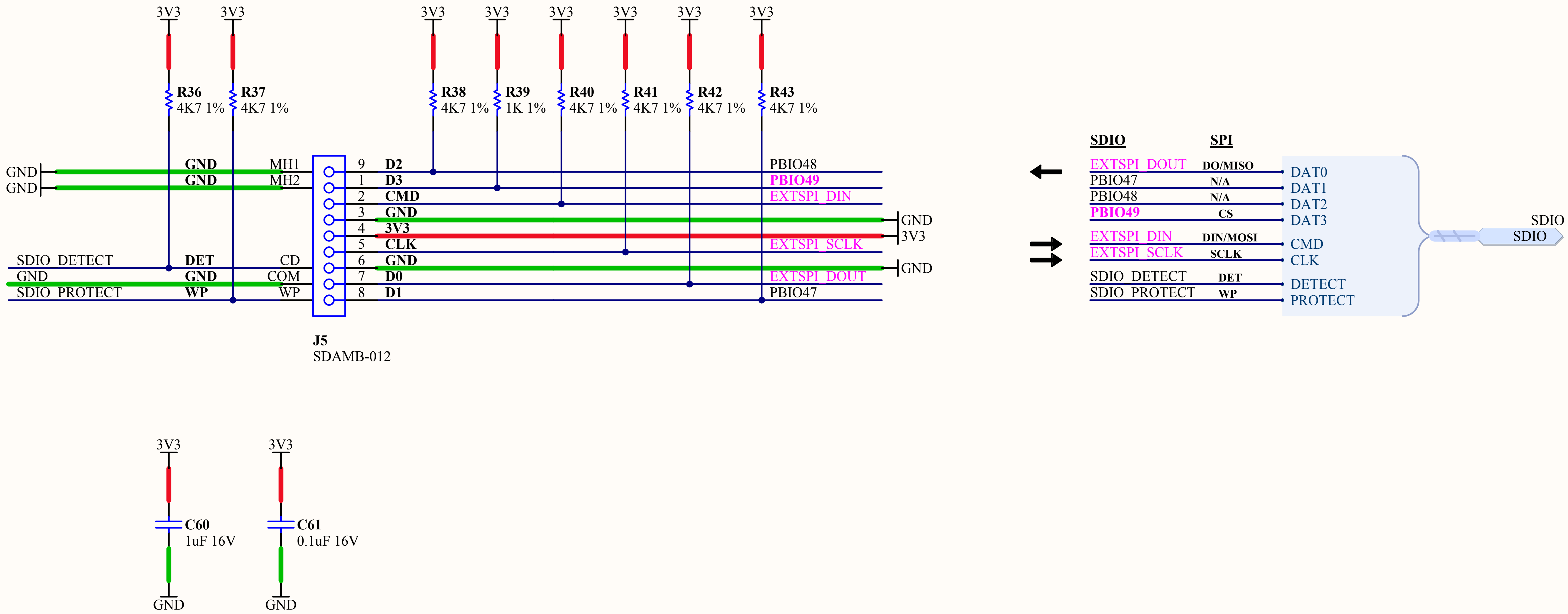
Colour level	0.83V	0.56V	0.27V	0.00V
MSB (1) 330R	1	1	0	0
LSB (0) 680R	1	0	1	0

TITLE: **SVGA 2BPP VIDEO PORT**
SIZE: A4 VERSION: CB500E CHKD: SRKH
DATE: 30/09/2009 TIME: 9:39:03 PM SHEET 13 OF 18
FILE: C:\AppleLogic\CarteBlanche\CB1_TEMPLATE\SVGA.SchDoc

www.AppleLogic.org
Carte Blanche
Apple II FPGA Peripheral Board



TITLE: **IDE INTERFACE**			www.AppleLogic.org
SIZE: **A4**	VERSION: **CB500E**	CHKD: **SRKH**	Carte Blanche
DATE: 30/09/2009	TIME: 9:39:03 PM	SHEET 14 OF 18	Apple II FPGA Peripheral Board
FILE: *C:\AppleLogic\CarteBlanche\CB1_TEMPLATE\IDE.SchDoc*			



TITLE: **SDIO INTERFACE**

SIZE: **A4** VERSION: **CB500E** CHKD: **SRKH**

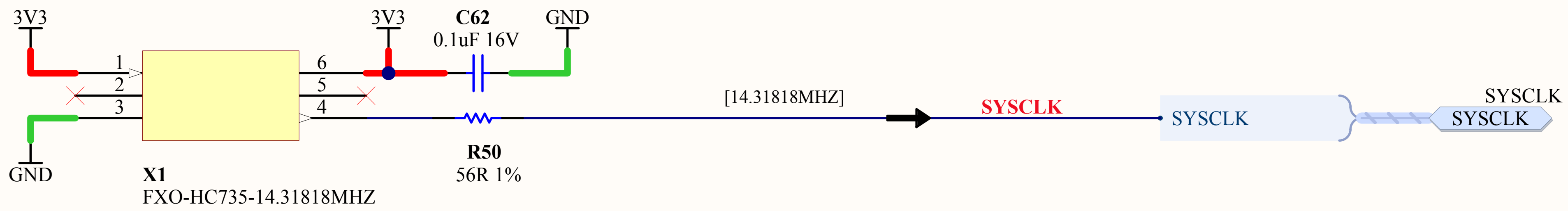
DATE: 30/09/2009 TIME: 9:39:03 PM SHEET 15 OF 18

FILE: *C:\AppleLogic\CarteBlanche\CB1_TEMPLATE\SDIO.SchDoc*

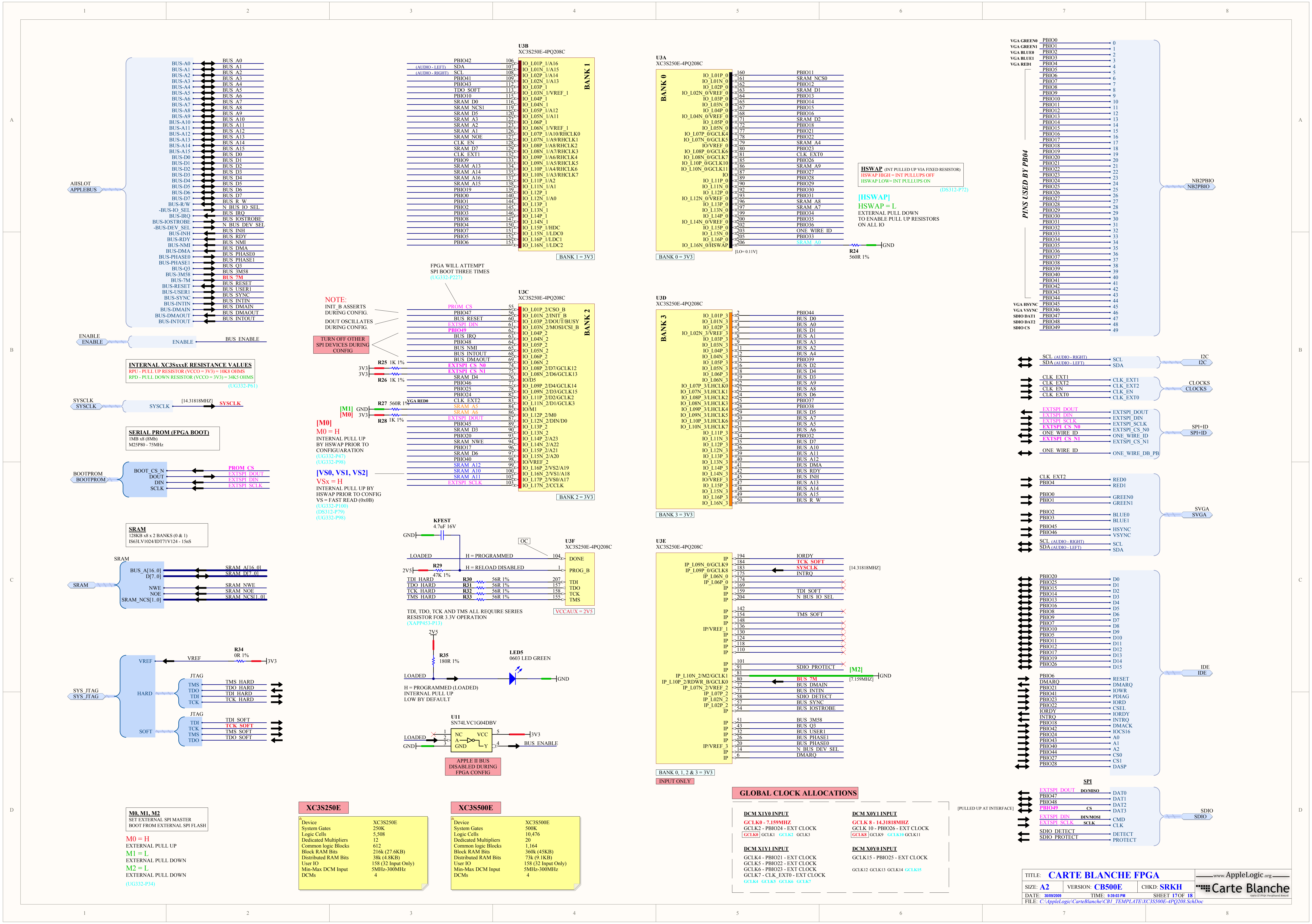
www.AppleLogic.org

Carte Blanche

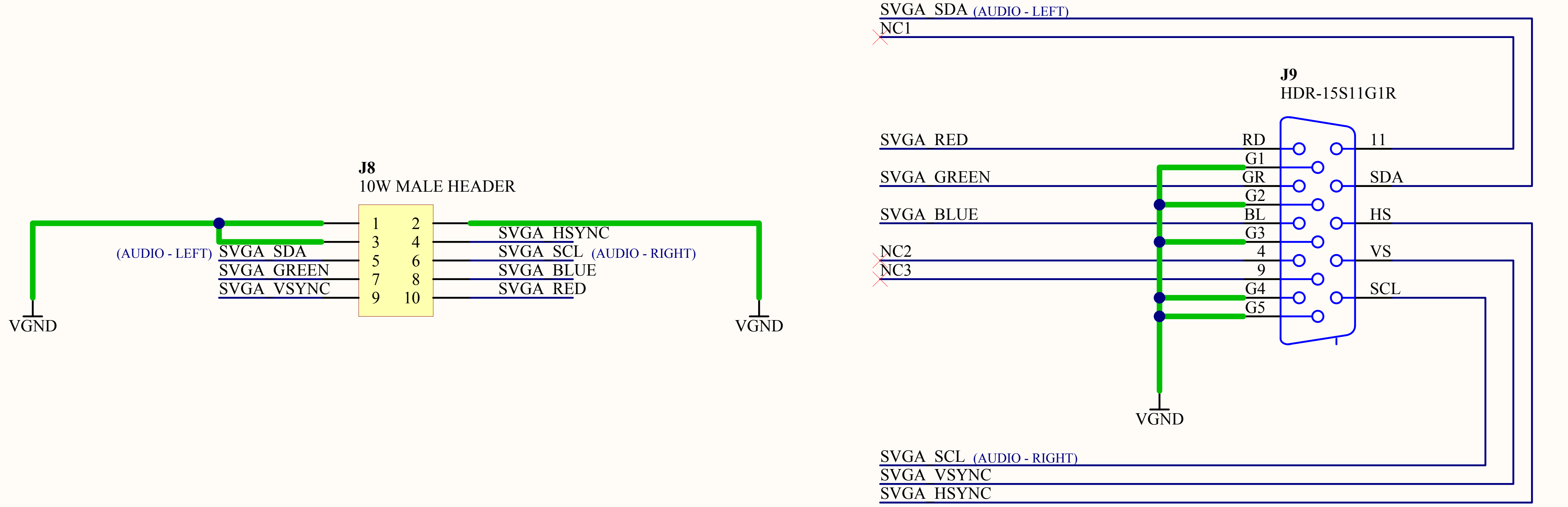
Apple II FPGA Peripheral Board



TITLE: 14.31818MHZ SYS CLOCK			www.AppleLogic.org Carte Blanche Apple II FPGA Peripheral Board
SIZE: A4	VERSION: CB500E	CHKD: SRKH	
DATE: 30/09/2009	TIME: 9:39:03 PM	SHEET 16 OF 18	
FILE: C:\AppleLogic\CarteBlanche\CB1_TEMPLATE\SYSCLK.SchDoc			



INTERNAL XC3SxxxE RESISTANCE VALUES
RPU - PULL UP RESISTOR (VCCO = 3V3) = 10K8 OHMS
RPD - PULL DOWN RESISTOR (VCCO = 3V3) = 34K5 OHMS
(UG332-P61)
SERIAL PROM (FPGA BOOT)
1MB x8 (8Mb)
M25P80 - 75MHz
SRAM
128KB x8 x 2 BANKS (0 & 1)
IS63LV1024/IDT71V124 - 15nS
NOTE:
INIT_B ASSERTS DURING CONFIG.
DOUT OSCILLATES DURING CONFIG.
TURN OFF OTHER SPI DEVICES DURING CONFIG
FPGA WILL ATTEMPT SPI BOOT THREE TIMES
(UG332-P227)
[M0]
M0 = H
INTERNAL PULL UP BY HSWAP PRIOR TO CONFIGURATION
(UG332-P47)
(UG332-P98)
[VS0, VS1, VS2]
VSx = H
INTERNAL PULL UP BY HSWAP PRIOR TO CONFIG
VS = FAST READ (0x0B)
(UG332-P100)
(DS312-P79)
(UG332-P98)
HSWAP (INT PULLED UP VIA FIXED RESISTOR)
HSWAP HIGH = INT PULLUPS OFF
HSWAP LOW= INT PULLUPS ON
(DS312-P72)
[HSWAP]
HSWAP = L
EXTERNAL PULL DOWN TO ENABLE PULL UP RESISTORS ON ALL IO
PINS USED BY PB04
TDI, TDO, TCK AND TMS ALL REQUIRE SERIES RESISTOR FOR 3.3V OPERATION
(XAPP453-P13)
H = PROGRAMMED (LOADED)
INTERNAL PULL UP
LOW BY DEFAULT
APPLE II BUS DISABLED DURING FPGA CONFIG
M0, M1, M2
SET EXTERNAL SPI MASTER
BOOT FROM EXTERNAL SPI FLASH
M0 = H
EXTERNAL PULL UP
M1 = L
EXTERNAL PULL DOWN
M2 = L
EXTERNAL PULL DOWN
(UG332-P34)
XC3S250E
Device XC3S250E
System Gates 250K
Logic Cells 5,508
Dedicated Multipliers 12
Common logic Blocks 612
Block RAM Bits 216k (27.6KB)
Distributed RAM Bits 38k (4.8KB)
User IO 158 (32 Input Only)
Min-Max DCM Input 5MHz-300MHz
DCMs 4
XC3S500E
Device XC3S500E
System Gates 500K
Logic Cells 10,476
Dedicated Multipliers 20
Common logic Blocks 1,164
Block RAM Bits 360k (45KB)
Distributed RAM Bits 73k (9.1KB)
User IO 158 (32 Input Only)
Min-Max DCM Input 5MHz-300MHz
DCMs 4
GLOBAL CLOCK ALLOCATIONS
DCM X1Y0 INPUT
GCLK0 - 7.159MHZ
GCLK2 - PBIO24 - EXT CLOCK
DCM X0Y1 INPUT
GCLK 8 - 14.31818MHZ
GCLK 10 - PBIO26 - EXT CLOCK
DCM X1Y1 INPUT
GCLK4 - PBIO21 - EXT CLOCK
GCLK5 - PBIO22 - EXT CLOCK
GCLK6 - PBIO23 - EXT CLOCK
GCLK7 - CLK_EXT0 - EXT CLOCK
DCM X0Y0 INPUT
GCLK15 - PBIO25 - EXT CLOCK
BANK 0, 1, 2 & 3 = 3V3
INPUT ONLY
VCCAUX = 2V5
TITLE: CARTE BLANCHE FPGA
SIZE: A2
VERSION: CB500E
CHKD: SRKH
DATE: 30/09/2009
TIME: 9:39:03 PM
SHEET 17 OF 18
FILE: C:\AppleLogic\CarteBlanche\CB1_TEMPLATE\XC3S500E-4PQ208.SchDoc
www.AppleLogic.org
Carte Blanche



SVGA INTERFACE

TITLE: AII SVGA MOUNTING BOARD		
SIZE: A4	VERSION: CB500E	CHKD: SRKH
DATE: 30/09/2009	TIME: 9:39:04 PM	SHEET 18 OF 18
FILE: C:\AppleLogic\CarteBlanche\CB1_TEMPLATE\SVGAIO.SchDoc		

www.AppleLogic.org
Carte Blanche
Apple II FPGA Peripheral Board