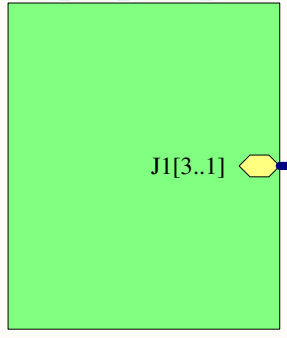


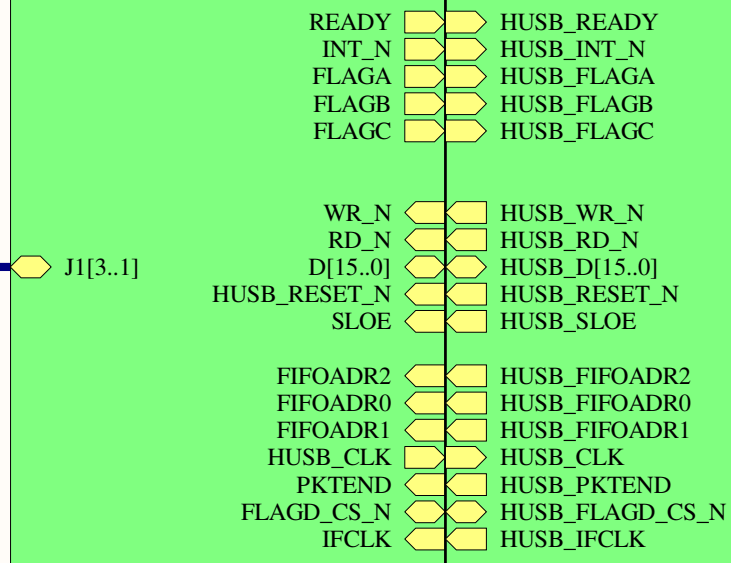
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XC3S500E-CP132.SchDoc

CON_USB_MINIB_RA.SchDoc
CON_USB_MINIB_RA.SchDoc

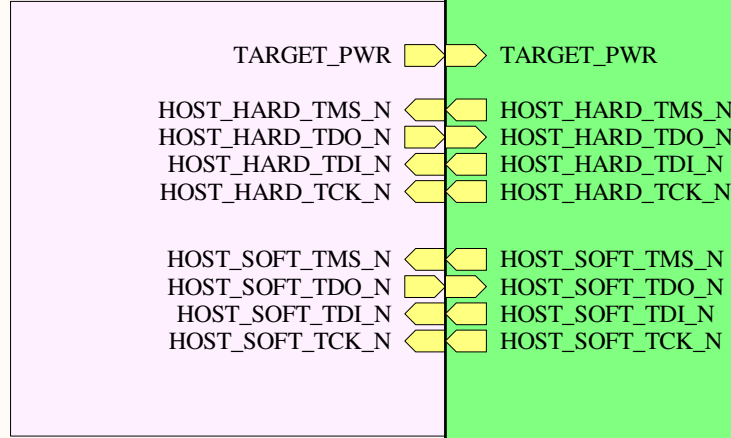


J1[3..1]

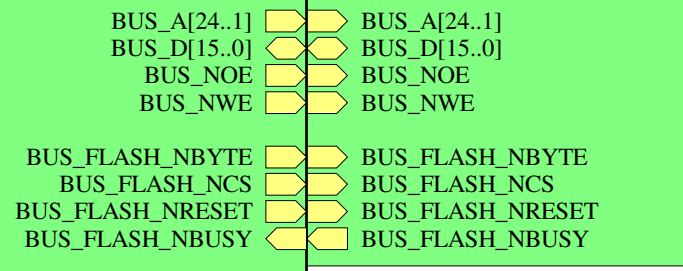
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USB_CY7C68001-56LFC_2.SchDoc



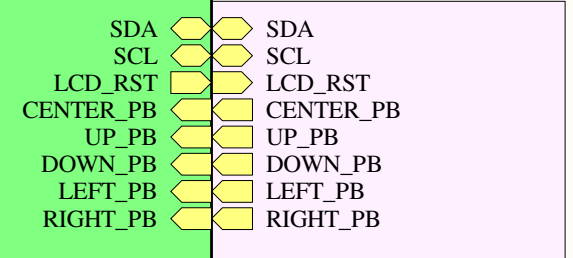
CON_IO_5
CON_10WBOXHDREDGEM.SchDoc



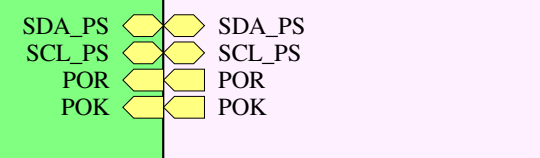
FLASH_1
FLASH_S29GL256N11FFIV10_16Mx16.SchDoc



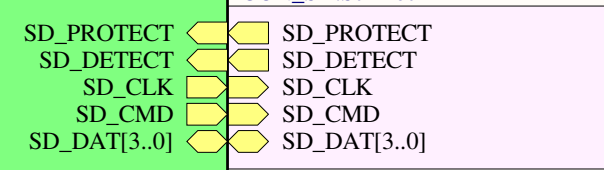
KEYPAD_1
LCD+SW.SCHDOC



POWERSUPPLY
POWERSUPPLY.SchDoc



CON_SD_1
CON_SD.SchDoc



△
== Steve's Gadget ==

Some features;

- High Speed standard JTAG organised as 4 differential pairs or 8 single ended I/O's
Soft configured as:
Hard JTAG - TMS,TDI,TCK,TDO
Soft JTAG - TMS,TDI,TCK,TDO
- Directly compatible with Altium products, compatible with other products with cable and adaptors.
- Is Automatically powered by the Altium NB2 SYSTEM JTAG port
- Acts a "Virtual Tool" in the NB2 "Debug ports A and B"
- JTAG Interface has IO voltage that can be software configured (Via I2C) for an interface voltage of either 1.8V, 2.5V or 3.3V
- High Speed USB (480MB/s) (16 bit interface) –Standard Cypress CY7C68001 transceiver)
- Adaptor is powered by either the USB interface or the Host JTAG Interface (Pin 9)
- Single on-board FLASH (32MB) for both FPGA config and soft core executable ROM + bit map storage (16 Bit Parallel Interface)
- SD Slot for either SD Memory card with FAT or Wireless Ethernet Card for remote operation (or Bluetooth)
- OLED Display for status and selection (104x16 pixels - I2C Interface)
- 5 way Joystick style menu navigation button (same as digital camera's) (up/down/left/right/center)
- General purpose ACTIVITY/ON Led Indicator (Green) next to USB connector
- DS2406 One Wire Device Identifies the product as an Altium product and allows various configurations.
- DS2406 also contains 1K of write only memory
- Low cost, small, 4 layer, top side only, single sided assembly design

Software Features;

- One touch programming of JTAG images
- Auto target detect using JTAG ID's or manual target select
ie - FLASH ROM or FPGA with Flash (XC3S E Series)
- Portable program library via SD card, or virtual library via Wireless SD Card

Sheet Title Serial JTAG Adapter		Project Organization	
Project Title ProjectTitle		ProjectAddress1	
Size: A4	Assy: ProjectAssyNum	Revision: ProjectRevision	ProjectAddress2
Date: 26/10/2007	Time: 4:31:03 PM	Common Sheet	ProjectAddress3
File: SJA01.01.SchDoc			ProjectAddress4



U1A
XC3S500E-4CP132C

BANK 0

IO	PU	HOST HARD	TDI N
IO_L01N_1/A13	PU	HOST HARD	TDI N
IO_L01P_1/A12	PU	HOST HARD	TCK N
IO_L02N_1/A12	PU	HOST HARD	TMS N
IO_L02P_1/A11	PU	HOST HARD	TMS N
IO_L03N_1/A11	PU	HOST SOFT	TDI N
IO_L03P_1/A10	PU	HOST SOFT	TDI N
IO_L04N_1/A10	PU	HOST SOFT	TCK N
IO_L04P_1/A9	PU	HOST SOFT	TCK N
IO_L05N_1/A9	PU	CENTER_PB	[CENTER]
IO_L05P_1/A8	PU	UP_PB	[UP]
IO_L06N_1/A8	PU	DOWN_PB	[DOWN]
IO_L06P_1/A7	PU	LEFT_PB	[LEFT]
IO_L07N_1/A7	PU	RIGHT_PB	[RIGHT]
IO_L07P_1/A6	PU	POK	[HIGH= POWER OK]
IO_L08N_1/A6	PD	SD_DETECT	[HIGH= SD CARD IN]
IO_L08P_1/A5	PD	SD_PROTECT	[LOW= SD WRITE PROTECT]
IO_L09N_1/A5	PD	FPGA_B0_C4	
IO_L09P_1/A4	PD	FPGA_B0_B4	
IO_L10N_1/A4	PD	FPGA_B0_A4	
IO_L10P_1/A3	PD	FPGA_B0_A3	
IO_L11N_1/A3	PD	FPGA_B0_A3	
IO_L11P_1/A2	PD	FPGA_B0_A3	

BANK 0 = 1V8/2V5/3V0

HSWAP (INT PULLED UP VIA FIXED RESISTOR)
HSWAP HIGH = INT PULLUPS OFF
HSWAP LOW = INT PULLUPS ON

U1C
XC3S500E-4CP132C

BANK 2

IO/D	M1	BUS D5
IO/D13	M1	BUS D5
IO/M1	INIT B	HUSB_FIFOADR0
IO/VREF_1	CS1 B	BUS D11
IO_L01N_2/INIT_1	LED	[LO=0.06V]
IO_L01P_2/CSO_1	D6	BUS D13
IO_L02N_2/MOSI/CSL_1	D7	BUS D6
IO_L02P_2/DOUT/BUSY_1	D3	BUS D3
IO_L03N_2/D6/GCLK1_1	D4	BUS D4
IO_L03P_2/D7/GCLK1_1	D1	BUS D1
IO_L04N_2/D3/GCLK1_1	D2	BUS D2
IO_L04P_2/D4/GCLK1_1	D0	BUS D0
IO_L06N_2/D1/GCLK1_1	PU M0	LCD_RST [LOW= LCD RESET]
IO_L06P_2/D2/GCLK1_1	A22	BUS A22
IO_L07N_2/DIN/D_1	A23	BUS A23
IO_L07P_2/M_1	A20	BUS A20
IO_L08N_2/A2	A21	BUS A21
IO_L08P_2/A2	A18	BUS A18
IO_L09N_2/A2	A19	BUS A19
IO_L09P_2/A2	A17	BUS A17
IO_L10N_2/VS1/A1_1	CCLK	BUS A24
IO_L10P_2/VS2/A1_1		
IO_L11N_2/CCLK_1		
IO_L11P_2/VS0/A1_1		

BANK 2 = 3V3

U1B
XC3S500E-4CP132C

BANK 1

IO/A	A0/D15	BUS D15
IO/A13	A15	BUS A15
IO/VREF_1	A16	BUS A16
IO_L01N_1/A13	A13	BUS A13
IO_L01P_1/A12	A14	BUS A14
IO_L02N_1/A12	A11	BUS A11
IO_L02P_1/A11	A12	BUS A12
IO_L03N_1/A11	A9	BUS A9
IO_L03P_1/A10	A10	BUS A10
IO_L04N_1/A9/RHCLK_1	A7	BUS A7
IO_L04P_1/A10/RHCLK_1	A8	BUS A8
IO_L05N_1/A7/RHCLK3/TRDY_1	A5	BUS A5
IO_L05P_1/A8/RHCLK_1	A6	BUS A6
IO_L06N_1/A5/RHCLK_1	A3	BUS A3
IO_L06P_1/A6/RHCLK4/IRDY_1	A4	BUS A4
IO_L07N_1/A3/RHCLK_1	A1	BUS A1
IO_L07P_1/A4/RHCLK_1	A2	BUS A2
IO_L08N_1/A1	PU LDC0	BUS_FLASH_NCS
IO_L08P_1/A1	HDC	BUS NWE
IO_L09N_1/LDC_1	LDC2	BUS_FLASH_NBYTE
IO_L09P_1/HDC_1	LDC1	BUS_NOE
IO_L10N_1/LDC_1		
IO_L10P_1/LDC_1		

BANK 1 = 3V3

LDC0 (INT PULL UP VIA HSWAP)
HSWAP WILL DISABLE CS OF BPI FLASH

BPI FLASH CONTROL

XC3S500E	DIR	BPIFLASH
LDC0	-->	CE#/CS#
LDC1	-->	OE#
LDC2	-->	BYTE#
HDC	-->	WE#
D[7..0]	<-->	D[7..0]
A[n..1]	-->	A[n..1]
A0	-->	DQ15/A-1
CS1_B	<--	PULL LOW
RDWR_B	<--	PULL LOW

U1D
XC3S500E-4CP132C

BANK 3

IO	HUSB RD N
IO/VREF_1	HUSB_PKTEND
IO_L01N_1	BUS D8
IO_L01P_1	HUSB_SLOE
IO_L02N_1	BUS D10
IO_L02P_1	BUS D12
IO_L03N_1	BUS D14
IO_L03P_1	HUSB_FLAGD_CS_N
IO_L04N_3/LHCLK_1	HUSB_IFCLK
IO_L04P_3/LHCLK_1	HUSB_FIFOADR2
IO_L05N_3/LHCLK3/IRDY_1	SDA [DATA]
IO_L05P_3/LHCLK_1	SCL [CLOCK]
IO_L06N_3/LHCLK_1	OWB
IO_L06P_3/LHCLK4/TRDY_1	SD_CLK
IO_L07N_3/LHCLK_1	SD_CMD
IO_L07P_3/LHCLK_1	SD_DAT0
IO_L08N_1	SD_DAT1
IO_L08P_1	SD_DAT2
IO_L09N_1	SD_DAT3
IO_L09P_1	HUSB_FLAGA

BANK 3 = 3V3

U1E
XC3S500E-4CP132C

BANK 3

IP	HUSB FLAGB
IP_L06P_0/GCLK8	GCLK9
IP_L06N_0/GCLK9	FPGA_CLK [24MHz]
IP/VREF_1	HUSB_FLAGC
IP_L05P_2/RDWR_B/GCLK0	RDWR B
IP_L05N_2/M2/GCLK1	M2
IP/VREF_2	HUSB_INT N
IP/VREF_3	HUSB_READY

BANK 3 = 3V3

M1 (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG

INIT B (INT PULLED UP VIA FIXED RESISTOR)
MUST BE PULLED HIGH DURING CONFIG

CS1 B
MUST BE PULLED LOW DURING CONFIG

M0 (INT PULL UP VIA HSWAP)
START ADD = 0x00_0000 INCREMENTING
START ADD = 0xFF_FFFF DECREMENTING

CCLK
DO NOT DRIVE CCLK
ROUTE CCLK WITH SIGNAL INTEGRITY

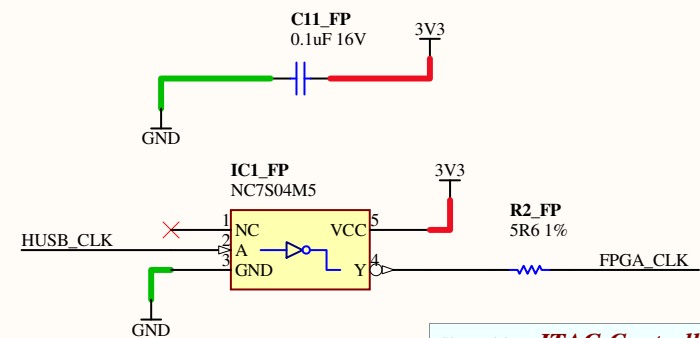
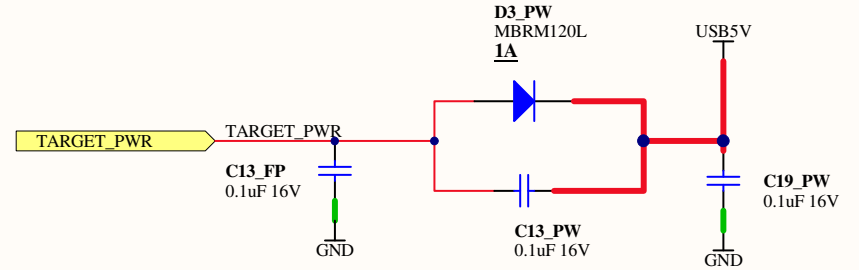
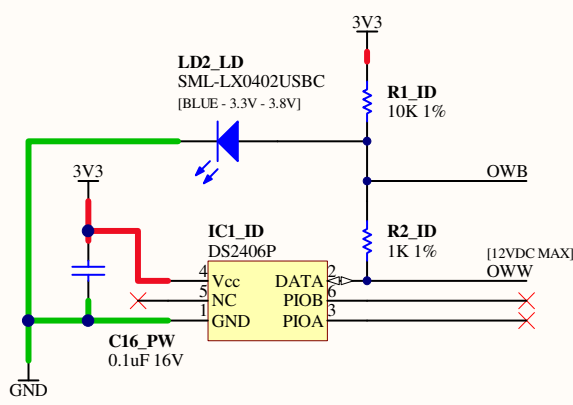
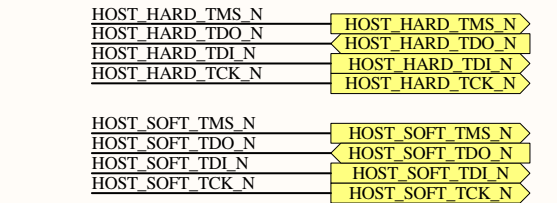
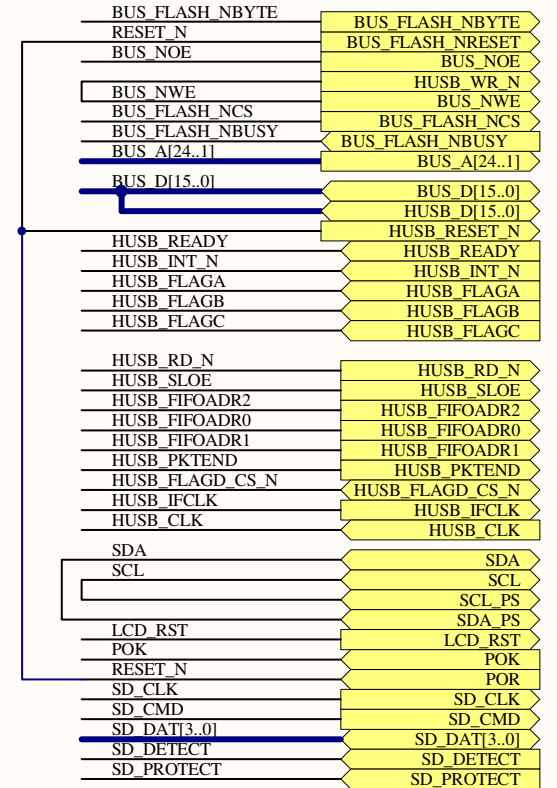
I2C DEVICES
DEV1 - UNIVISION - LCD - UG-0416ALBAG01
DEV2 - MAXIM - PSU - MAX8588ETM

GCLK9
FPGA SYSTEM CLOCK IS ON GLOBAL CLOCK 9

RDWR B
MUST BE PULLED LOW DURING CONFIG

M2 (INT PULL UP VIA HSWAP)
MUST BE PULLED LOW DURING CONFIG

INTERNAL XC3SxxxE RESISTANCE VALUES
RPU - PULL UP RESISTOR (VCCO = 3V3) = 10K8 OHMS
RPD - PULL DOWN RESISTOR (VCCO = 3V3) = 34K5 OHMS



1

2

3

4

A

A

B

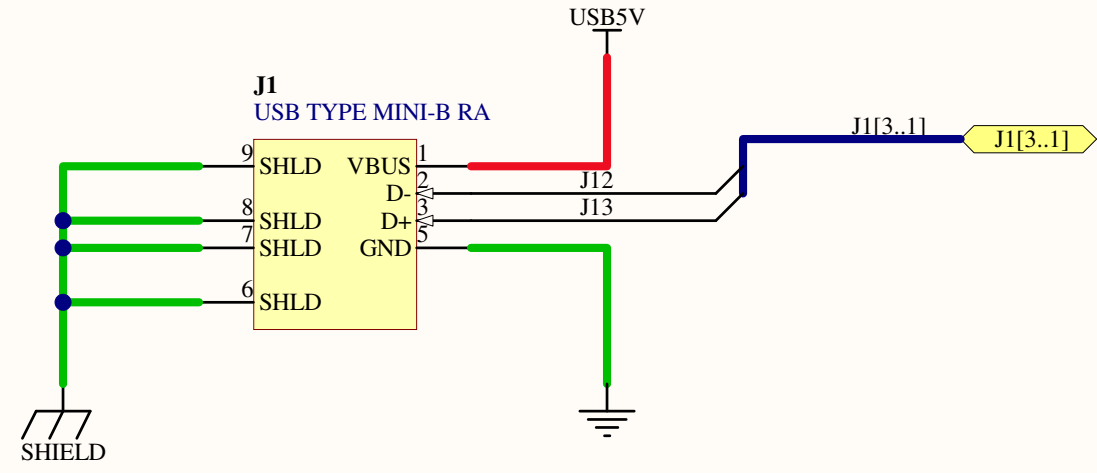
B

C

C

D

D



Sheet Title CON_USB_1		Project Organization	
Project Title ProjectTitle		ProjectAddress1	
Size: A4		ProjectAddress2	
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Date: 26/10/2007	Time: 4:31:03 PM	ProjectAddress4	
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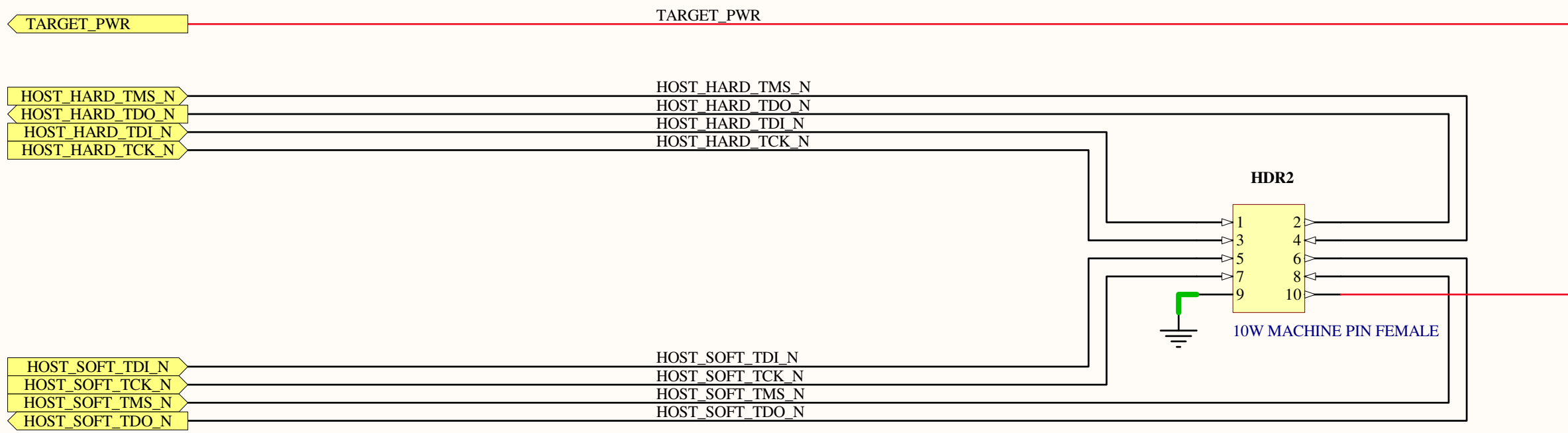


1

2

3

4

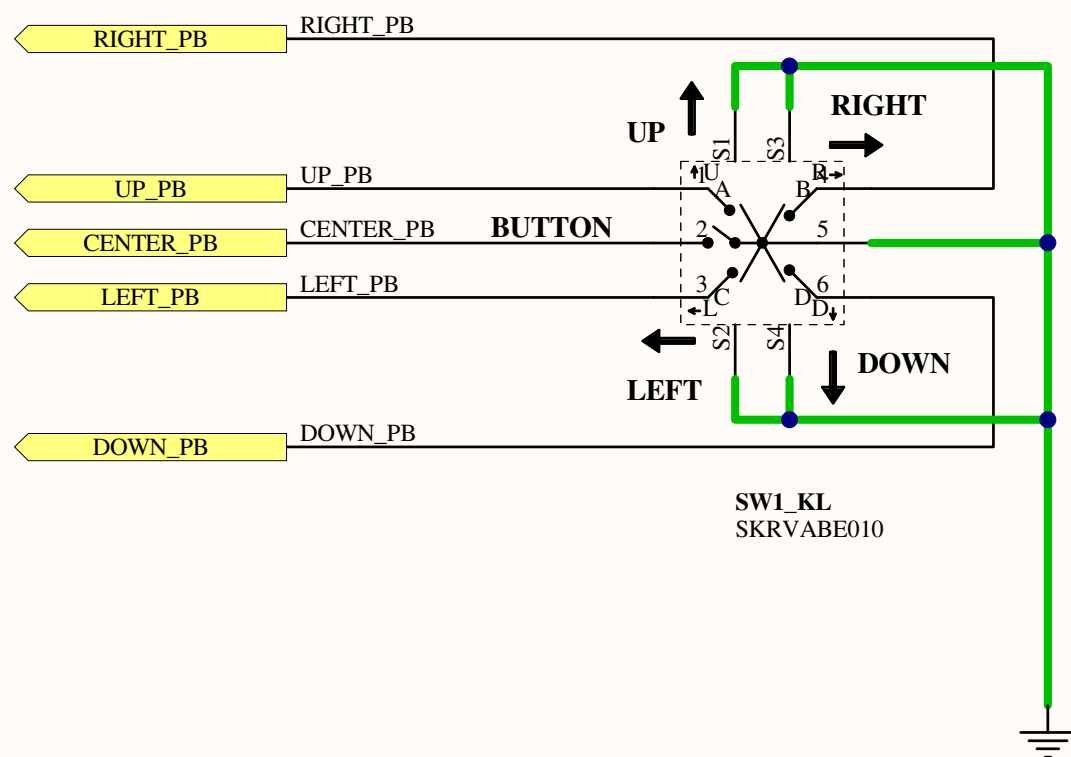


JTAG PROGRAMMING INTERFACE

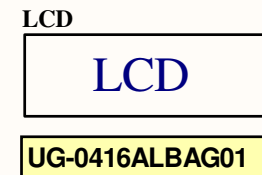
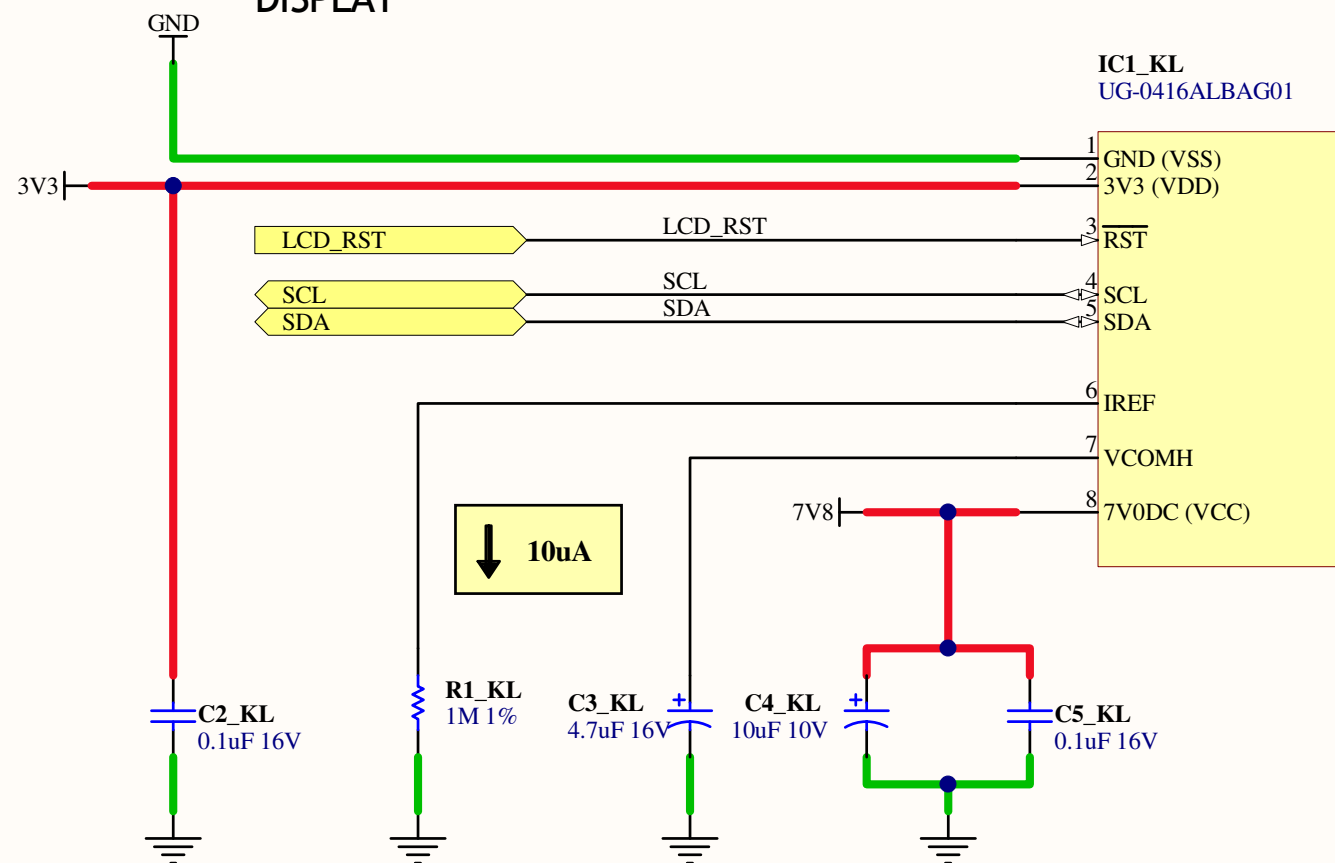
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KEYPAD



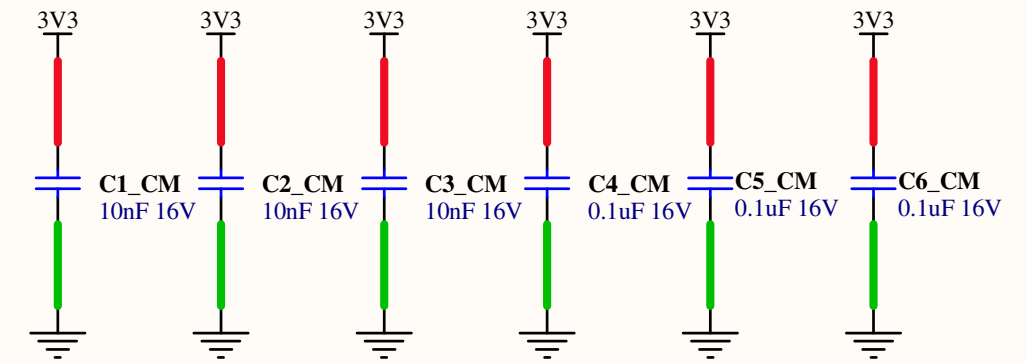
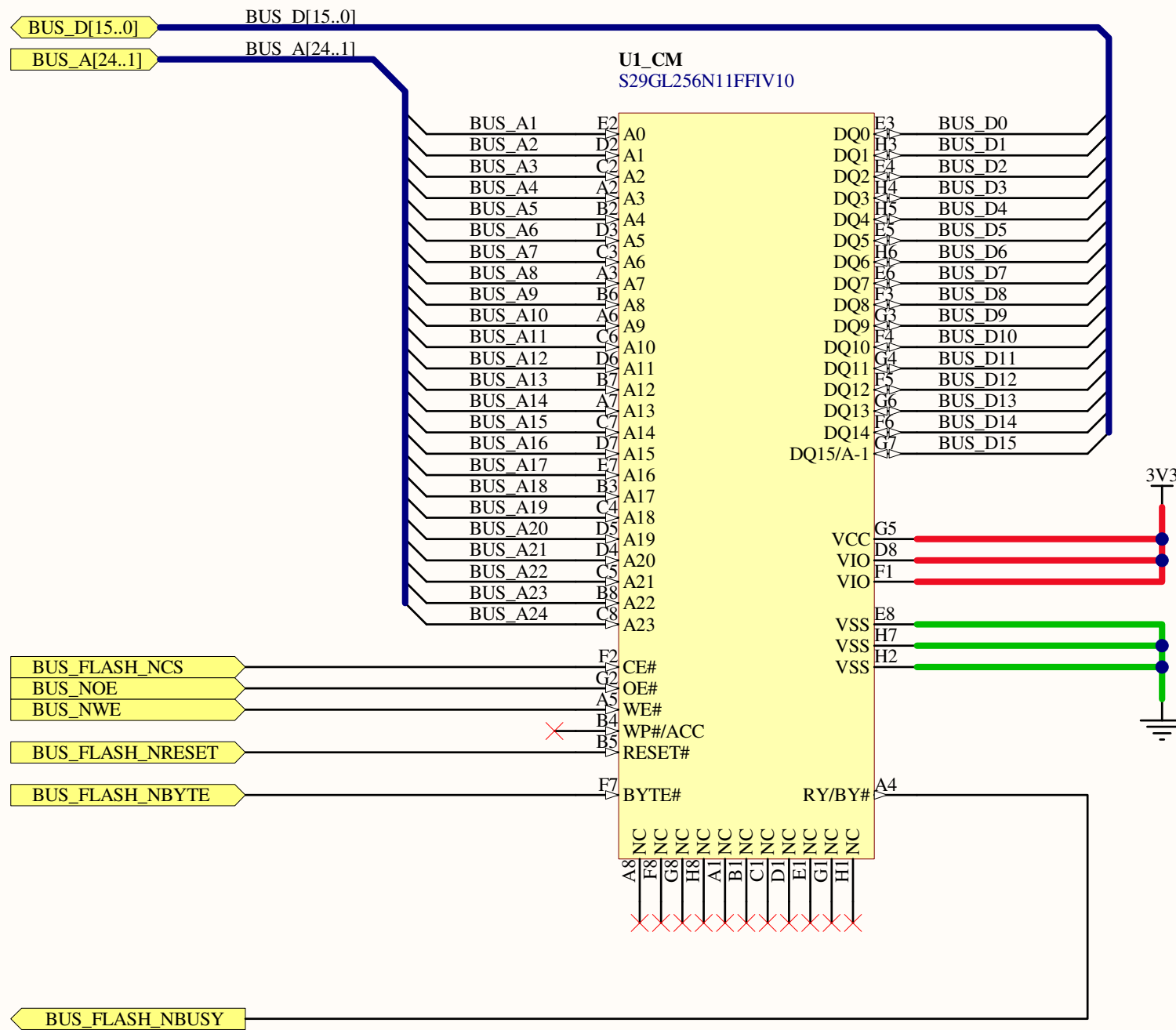
DISPLAY



IC1_KL
UG-0416ALBAG01

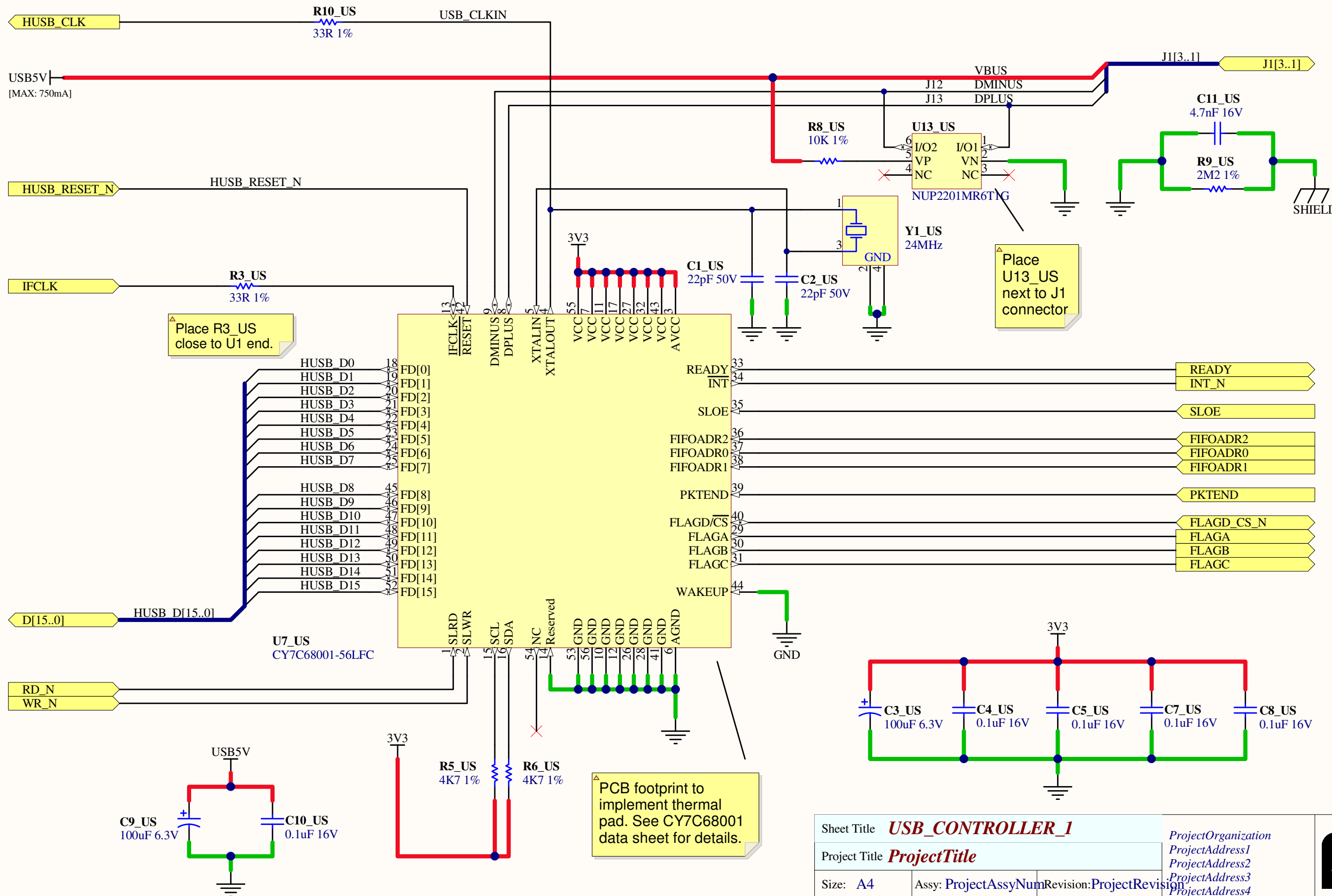
Sheet Title Control Key and LCD Display		Project Organization
Project Title ProjectTitle		ProjectAddress1
Size: A4	Assy: ProjectAssyNum	ProjectAddress2
Date: 26/10/2007	Time: 4:31:04 PM	ProjectAddress3
File: LCD+SW.SchDoc	Revision: ProjectRevision	ProjectAddress4
Common Sheet		





Sheet Title FLASH_1		Project Organization	
Project Title ProjectTitle		ProjectAddress1	
Size: A4	Assy: ProjectAssyNum	Revision: ProjectRevision	ProjectAddress2
Date: 26/10/2007	Time: 4:31:04 PM	Common Sheet	ProjectAddress3
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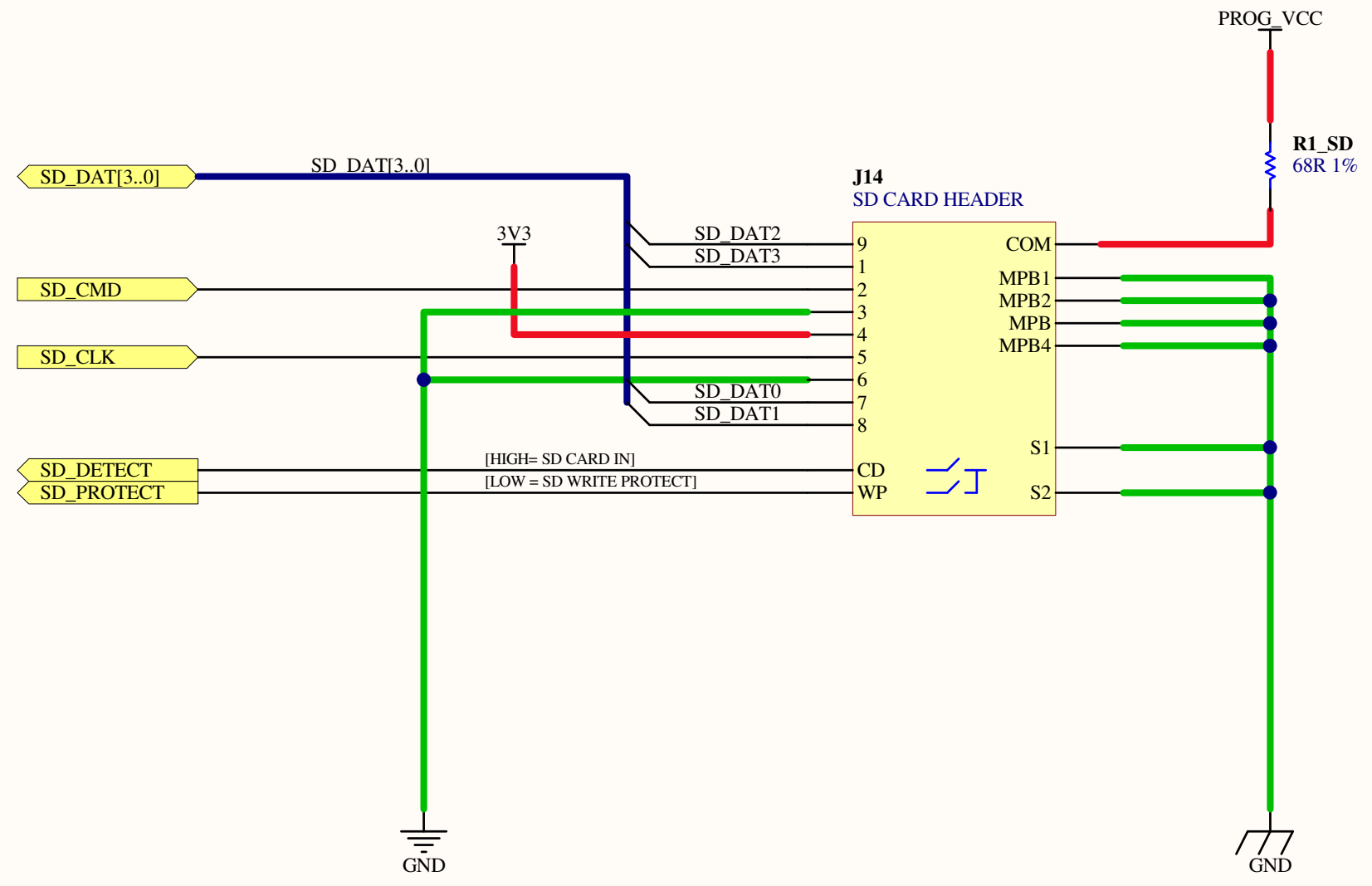
Place R3_US close to U1 end.

Place U13_US next to J1 connector

PCB footprint to implement thermal pad. See CY7C68001 data sheet for details.

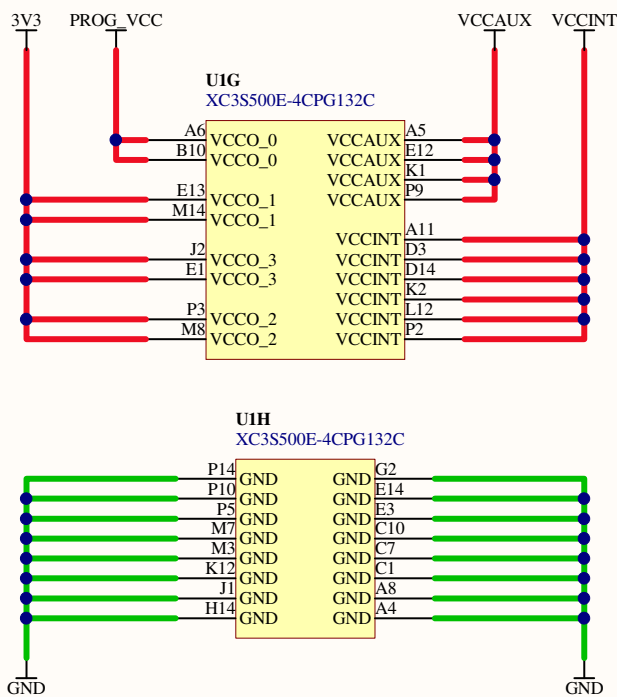
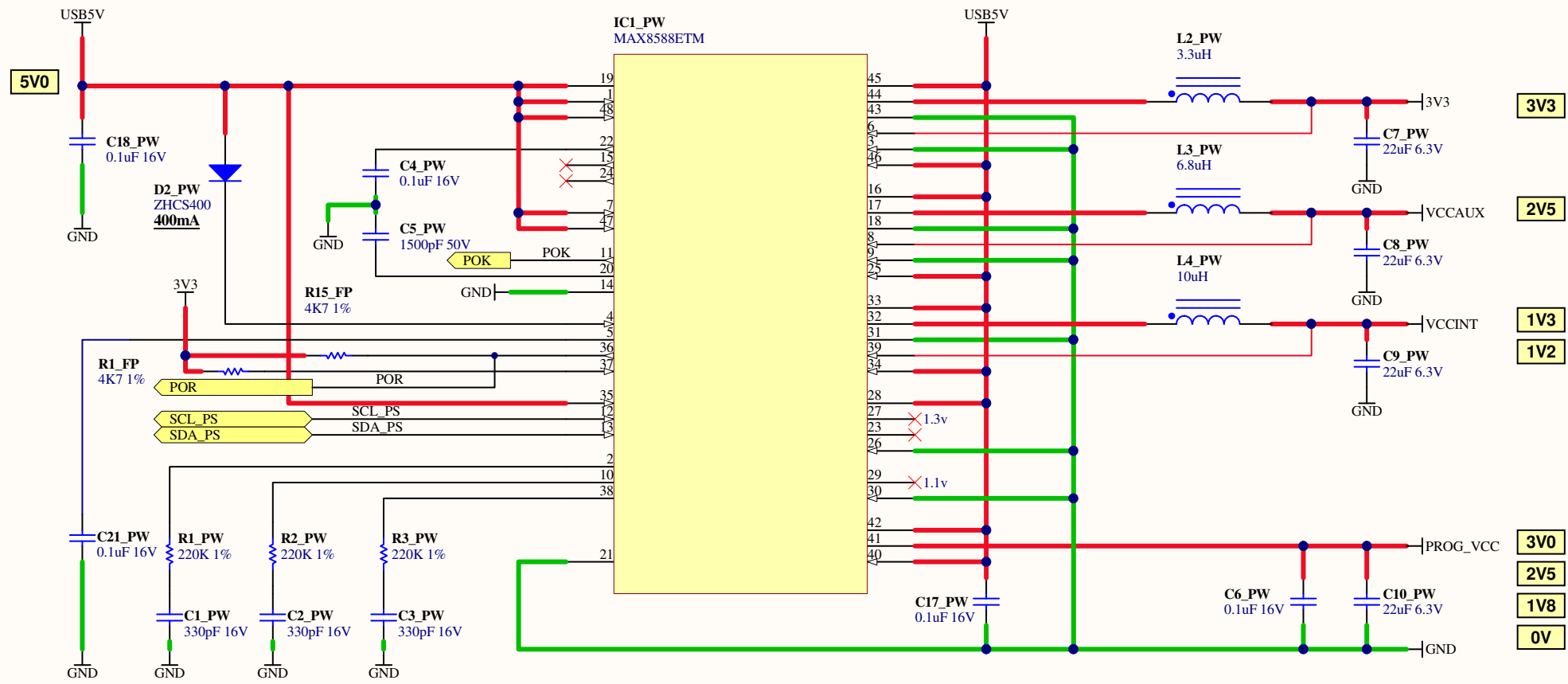
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Project Title ProjectTitle		ProjectAddress1	
Size: A4		ProjectAddress2	
Assy: ProjectAssyNum		ProjectAddress3	
Revision: ProjectRevision		ProjectAddress4	
Date: 26/10/2007	Time: 4:31:04 PM	Common Sheet	
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Sheet Title CON_SD_1		Project Organization	
Project Title ProjectTitle		ProjectAddress1	
Size: A4	Assy: ProjectAssyNum	Revision: ProjectRevision	ProjectAddress2
Date: 26/10/2007	Time: 4:31:04 PM	Common Sheet	ProjectAddress3
File: CON_SD.SchDoc			ProjectAddress4





POR REQUIREMENTS:
 1. - VCCINT - 1.2V
 2. - VCCAUX - 2.5V
 3. - VCCO BANK2 - 3.3V

