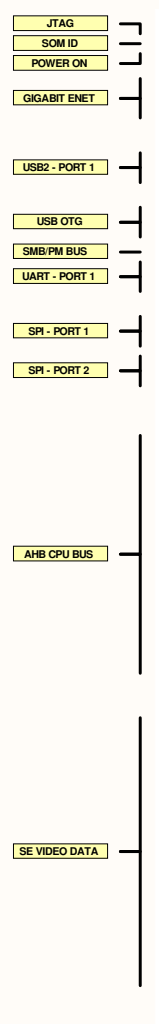
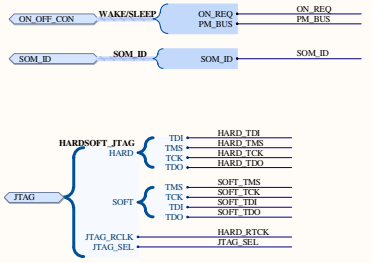
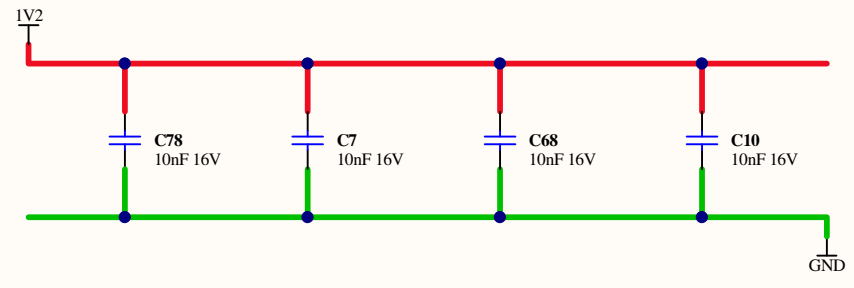
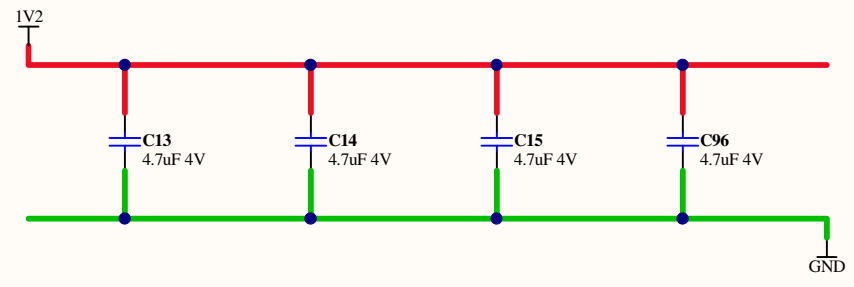
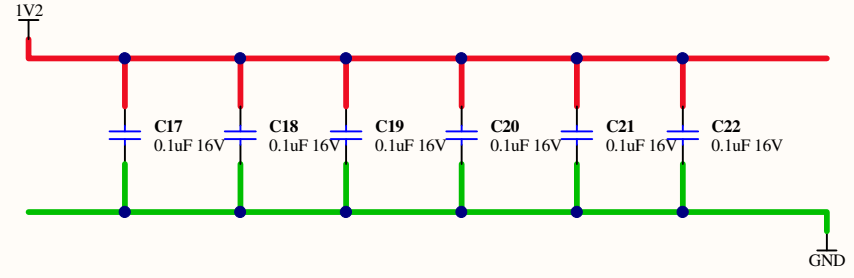


PCB1
SOM03 Blank PCB
Printed Circuit Board (Bare)

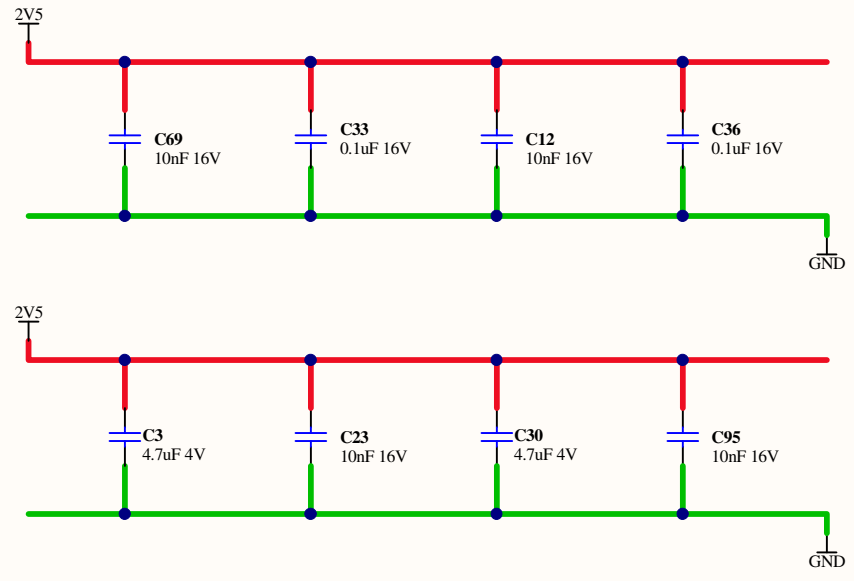
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Size	Number	Revision
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Date:	23/09/2011	Sheet of
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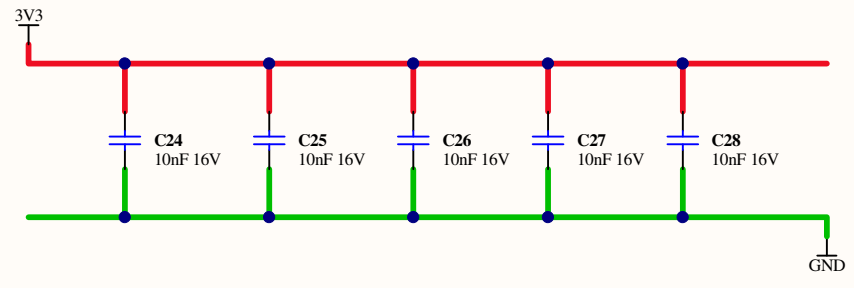
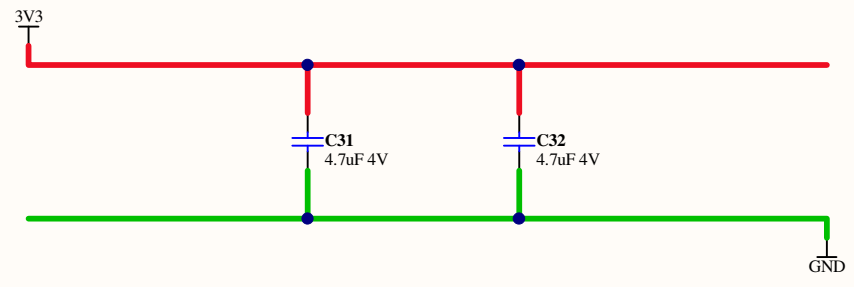
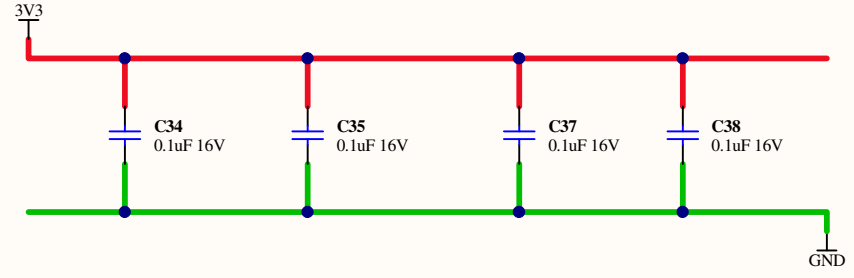
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JTAG_TDI	HARD_TDI	1	JTAG_TDI	JTAG_TDI	2	HARD_TDI	JTAG_TDI	1
JTAG_TCK	HARD_TCK	2	JTAG_TCK	JTAG_TCK	3	HARD_TCK	JTAG_TCK	2
SOM_ID	SOM_ID	3	JTAG_SEL	JTAG_SEL	4	JTAG_SEL	JTAG_SEL	3
ON_REQ	ON_REQ	4	MOD_WAKE	MOD_WAKE	5	ENET_Bp	ENET_Bp	4
ENET_Ap	ENET_Ap	5	GND	GND	6	GND	GND	5
ENET_Bn	FPGA_I01	6	FPGA_I01	FPGA_I01	7	FPGA_I01	FPGA_I01	6
GND	FPGA_I02	7	FPGA_I02	FPGA_I02	8	FPGA_I02	FPGA_I02	7
ENET_Cp	GND	8	FPGA_I03	FPGA_I03	9	GND	ENET_Dp	8
ENET_Cn	FPGA_I04	9	FPGA_I04	FPGA_I04	10	FPGA_I04	FPGA_I04	9
GND	FPGA_I05	10	FPGA_I05	FPGA_I05	11	FPGA_I05	FPGA_I05	10
GND	FPGA_I06	11	FPGA_I06	FPGA_I06	12	FPGA_I06	FPGA_I06	11
+B	GND	12	FPGA_I07	FPGA_I07	13	GND	+B	12
+B	GND	13	FPGA_I08	FPGA_I08	14	GND	+B	13
US2B_1_VBUS	FPGA_I09	14	FPGA_I09	FPGA_I09	15	FPGA_I09	FPGA_I09	14
US2B_1_DP	PWR_OUT11	15	PWR_SW	PWR_SW	16	PWR_SW	PWR_SW	15
US2B_1_Dn	GND	16	FPGA_I10	FPGA_I10	17	FPGA_I10	FPGA_I10	16
US2B1G_Dp	FPGA_I11	17	FPGA_I11	FPGA_I11	18	FPGA_I11	FPGA_I11	17
US2B1G_Dn	FPGA_I12	18	FPGA_I12	FPGA_I12	19	FPGA_I12	FPGA_I12	18
US2B1G_VBUS	PWR_OUT13	19	FPGA_I13	FPGA_I13	20	FPGA_I13	FPGA_I13	19
US2B1G_VBUS	PWR_OUT14	20	FPGA_I14	FPGA_I14	21	FPGA_I14	FPGA_I14	20
PM_BUS	FPGA_I15	21	FPGA_I15	FPGA_I15	22	FPGA_I15	FPGA_I15	21
UART1_TXD	PM_BUS	22	PM_BUS	PM_BUS	23	PM_BUS	PM_BUS	22
UART1_RTS	SOFT_TSD0	23	SOFT_TSD0	SOFT_TSD0	24	SOFT_TSD0	SOFT_TSD0	23
UART1_RXD	SOFT_TMS	24	SOFT_TMS	SOFT_TMS	25	SOFT_TMS	SOFT_TMS	24
UART1_CTS	SOFT_TDI	25	SOFT_TDI	SOFT_TDI	26	SOFT_TDI	SOFT_TDI	25
GND	SOFT_TDO	26	SOFT_TCK	SOFT_TCK	27	SOFT_TCK	SOFT_TCK	26
SPI1_TXD	GND	27	SOFT_TCK	SOFT_TCK	28	SOFT_TCK	SOFT_TCK	27
SPI1_RXD	FPGA_I01	28	FPGA_I01	FPGA_I01	29	FPGA_I01	FPGA_I01	28
SPI1_CLK	FPGA_I02	29	FPGA_I02	FPGA_I02	30	FPGA_I02	FPGA_I02	29
SPI1_CS	FPGA_I03	30	FPGA_I03	FPGA_I03	31	FPGA_I03	FPGA_I03	30
SPI2_TXD	FPGA_I04	31	FPGA_I04	FPGA_I04	32	FPGA_I04	FPGA_I04	31
SPI2_RXD	FPGA_I05	32	FPGA_I05	FPGA_I05	33	FPGA_I05	FPGA_I05	32
SPI2_CLK	FPGA_I06	33	FPGA_I06	FPGA_I06	34	FPGA_I06	FPGA_I06	33
SPI2_CS	FPGA_I07	34	FPGA_I07	FPGA_I07	35	FPGA_I07	FPGA_I07	34
GND	FPGA_I08	35	FPGA_I08	FPGA_I08	36	FPGA_I08	FPGA_I08	35
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+B	GND	37	FPGA_I10	FPGA_I10	38	GND	+B	37
+B	GND	38	FPGA_I11	FPGA_I11	39	GND	+B	38
+B	GND	39	FPGA_I12	FPGA_I12	40	GND	+B	39
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BUS_A1	FPGA_I02	41	FPGA_I14	FPGA_I14	42	FPGA_I14	FPGA_I14	41
BUS_A2	FPGA_I03	42	FPGA_I15	FPGA_I15	43	FPGA_I15	FPGA_I15	42
BUS_A3	FPGA_I04	43	FPGA_I16	FPGA_I16	44	FPGA_I16	FPGA_I16	43
BUS_A4	FPGA_I05	44	FPGA_I17	FPGA_I17	45	FPGA_I17	FPGA_I17	44
BUS_A5	FPGA_I06	45	FPGA_I18	FPGA_I18	46	FPGA_I18	FPGA_I18	45
BUS_A6	FPGA_I07	46	FPGA_I19	FPGA_I19	47	FPGA_I19	FPGA_I19	46
BUS_A7	FPGA_I08	47	FPGA_I20	FPGA_I20	48	FPGA_I20	FPGA_I20	47
BUS_A8	FPGA_I09	48	FPGA_I21	FPGA_I21	49	FPGA_I21	FPGA_I21	48
BUS_A9	FPGA_I10	49	FPGA_I22	FPGA_I22	50	FPGA_I22	FPGA_I22	49
BUS_A10	FPGA_I11	50	FPGA_I23	FPGA_I23	51	FPGA_I23	FPGA_I23	50
BUS_A11	FPGA_I12	51	FPGA_I24	FPGA_I24	52	FPGA_I24	FPGA_I24	51
BUS_A12	FPGA_I13	52	FPGA_I25	FPGA_I25	53	FPGA_I25	FPGA_I25	52
BUS_A13	FPGA_I14	53	FPGA_I26	FPGA_I26	54	FPGA_I26	FPGA_I26	53
BUS_A14	FPGA_I15	54	FPGA_I27	FPGA_I27	55	FPGA_I27	FPGA_I27	54
BUS_A15	FPGA_I16	55	FPGA_I28	FPGA_I28	56	FPGA_I28	FPGA_I28	55
GND	FPGA_I17	56	FPGA_I29	FPGA_I29	57	FPGA_I29	FPGA_I29	56
BUS_A16	GND	57	FPGA_I30	FPGA_I30	58	FPGA_I30	FPGA_I30	57
BUS_A17	FPGA_I01	58	FPGA_I31	FPGA_I31	59	FPGA_I31	FPGA_I31	58
BUS_A18	FPGA_I02	59	FPGA_I32	FPGA_I32	60	FPGA_I32	FPGA_I32	59
BUS_A19	FPGA_I03	60	FPGA_I33	FPGA_I33	61	FPGA_I33	FPGA_I33	60
BUS_A20	FPGA_I04	61	FPGA_I34	FPGA_I34	62	FPGA_I34	FPGA_I34	61
BUS_A21	FPGA_I05	62	FPGA_I35	FPGA_I35	63	FPGA_I35	FPGA_I35	62
BUS_A22	FPGA_I06	63	FPGA_I36	FPGA_I36	64	FPGA_I36	FPGA_I36	63
BUS_A23	FPGA_I07	64	FPGA_I37	FPGA_I37	65	FPGA_I37	FPGA_I37	64
BUS_A24	FPGA_I08	65	FPGA_I38	FPGA_I38	66	FPGA_I38	FPGA_I38	65
BUS_A25	FPGA_I09	66	FPGA_I39	FPGA_I39	67	FPGA_I39	FPGA_I39	66
BUS_A26	FPGA_I10	67	FPGA_I40	FPGA_I40	68	FPGA_I40	FPGA_I40	67
BUS_A27	FPGA_I11	68	FPGA_I41	FPGA_I41	69	FPGA_I41	FPGA_I41	68
BUS_A28	FPGA_I12	69	FPGA_I42	FPGA_I42	70	FPGA_I42	FPGA_I42	69
BUS_A29	FPGA_I13	70	FPGA_I43	FPGA_I43	71	FPGA_I43	FPGA_I43	70
BUS_A30	FPGA_I14	71	FPGA_I44	FPGA_I44	72	FPGA_I44	FPGA_I44	71
BUS_A31	FPGA_I15	72	FPGA_I45	FPGA_I45	73	FPGA_I45	FPGA_I45	72
BUS_A32	FPGA_I16	73	FPGA_I46	FPGA_I46	74	FPGA_I46	FPGA_I46	73
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BUS_A36	FPGA_I20	77	FPGA_I50	FPGA_I50	78	FPGA_I50	FPGA_I50	77
BUS_A37	FPGA_I21	78	FPGA_I51	FPGA_I51	79	FPGA_I51	FPGA_I51	78
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BUS_A45	FPGA_I29	86	FPGA_I59	FPGA_I59	87	FPGA_I59	FPGA_I59	86
BUS_A46	FPGA_I30	87	FPGA_I60	FPGA_I60	88	FPGA_I60	FPGA_I60	87
BUS_A47	FPGA_I31	88	FPGA_I61	FPGA_I61	89	FPGA_I61	FPGA_I61	88
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BUS_A86	FPGA_I70	127	FPGA_I100	FPGA_I100	128	FPGA_I100	FPGA_I100	127
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BUS_A88	FPGA_I72	129	FPGA_I102	FPGA_I102	130	FPGA_I102	FPGA_I102	129
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BUS_A90	FPGA_I74	131	FPGA_I104	FPGA_I104	132	FPGA_I104	FPGA_I104	131
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BUS_A98	FPGA_I82	139	FPGA_I112	FPGA_I112	140	FPGA_I112	FPGA_I112	139
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BUS_A102	FPGA_I86	143	FPGA_I116	FPGA_I116	144	FPGA_I116	FPGA_I116	143
BUS_A103	FPGA_I87	144	FPGA_I117	FPGA_I117	145	FPGA_I117	FPGA_I117	144
BUS_A104	FPGA_I88	145	FPGA_I118	FPGA_I118	146	FPGA_I118	FPGA_I118	145
BUS_A105	FPGA_I89	146	FPGA_I119	FPGA_I119	147	FPGA_I119	FPGA_I119	146
BUS_A106	FPGA_I90	147	FPGA_I120	FPGA_I120	148	FPGA_I120	FPGA_I120	147
BUS_A107	FPGA_I91	148	FPGA_I121	FPGA_I121	149	FPGA_I121	FPGA_I121	148
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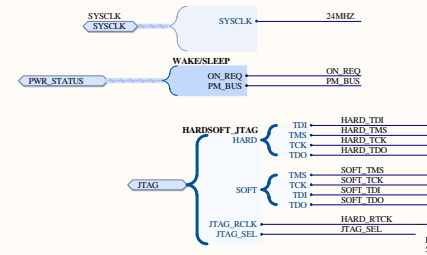
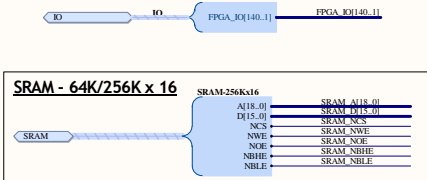
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Sheet Title FPGA Bypass 2V5		<i>Altium Limited</i> 3 Minna Close Belrose NSW 2085 Australia		
Project Title SOM02				
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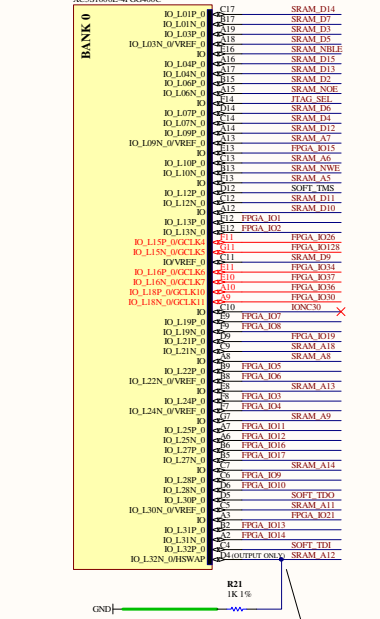


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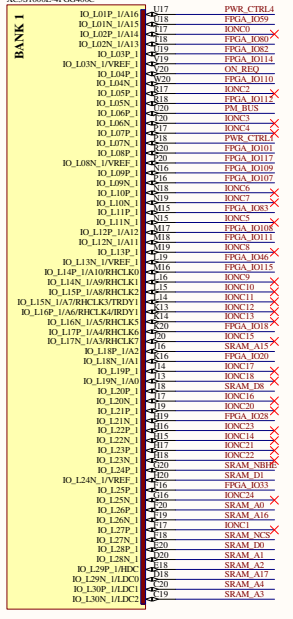


GCLK0
FPGA SYSTEM CLOCK IS ON GLOBAL CLOCK @ 24MHz

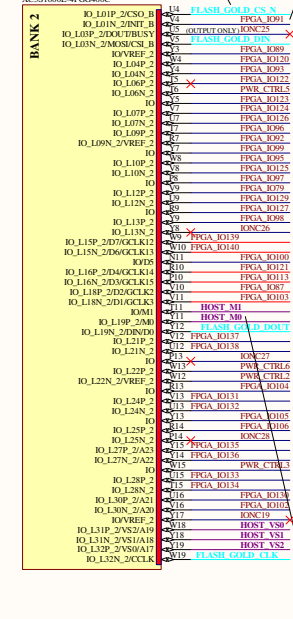
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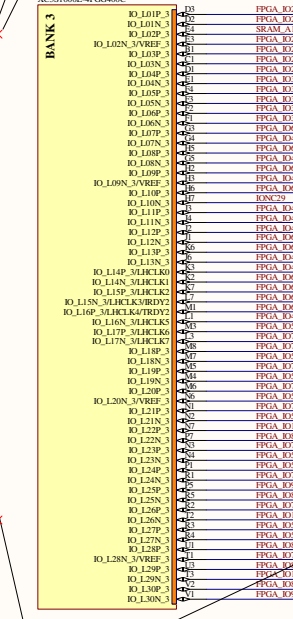
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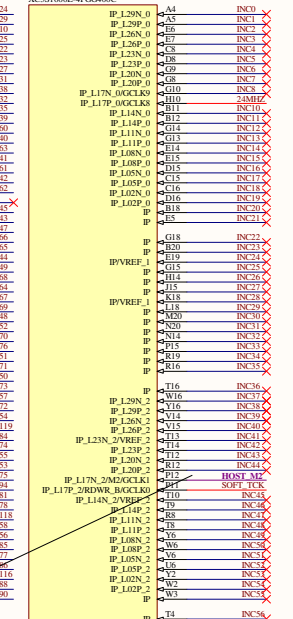
U3C
XC3S1600E-4FGG400C



U3D
XC3S1600E-4FGG400C



U3E
XC3S1600E-4FGG400C



[HSWAP]
HSWAP (INT PULLED UP VIA FIXED RESISTOR)
HSWAP HIGH - INT PULLUPS OFF
HSWAP LOW - INT PULLUPS ON (UG332-P27)

[HSWAP]
HSWAP = L
EXTERNAL PULL DOWN TO ENABLE PULL UP RESISTORS ON ALL IO

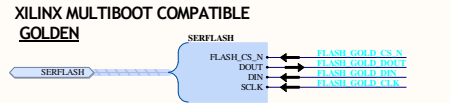
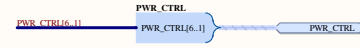
INTERNAL XC3S1600E RESISTANCE VALUES
RPU - PULL UP RESISTOR (VCC0 - V_I) = 100k OHMS
RPD - PULL DOWN RESISTOR (VCC0 - V_I) = 34k5 OHMS

1V2
FPGA DECOUPLING CAPS_1V2
FPGA_Bypass_FPGA_1V2.SchDoc

2V5
FPGA DECOUPLING CAPS_2V5
FPGA_Bypass_FPGA_2V5.SchDoc

3V3
FPGA DECOUPLING CAPS_3V3
FPGA_Bypass_FPGA_3V3.SchDoc

NOTE:
INT B ASSERTS DURING CONFIG.
SPI BOOT THREE TIMES (UG332-P227)
DOUT OSCILLATES DURING CONFIG.



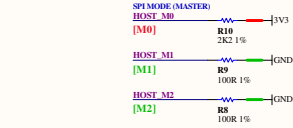
XC3S1600E MODE PIN CONFIGURATIONS

M0	M1	M2	FUNCTION
0	0	0	PLATFORM FLASH MODE
0	0	1	SPI MASTER (MASTER)
0	1	0	BYTE PARALLEL INTERFACE
0	1	1	INTERNAL MASTER SPI FLASH
1	0	0	-RESERVED-
1	0	1	JTAG MODE
1	1	0	SLAVE PARALLEL
1	1	1	SLAVE SERIAL

XC3S1600E SPI MODE CONFIGURATIONS

M0	M1	M2	FUNCTION
0	0	0	-RESERVED-
0	0	1	-RESERVED-
0	1	0	-RESERVED-
0	1	1	(000) STANDARD READ
1	0	0	(000) READ ARBITRARY
1	1	0	(000) SPI FAST READ
1	1	1	(000) SPI FAST READ

[M0]
M0 = H
INTERNAL PULL UP BY HSWAP PRIOR TO CONFIGURATION (UG332-P9)



M0 (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
EXT SPI BOOT MODE (MASTER)

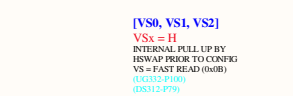
M1 (INT PULL UP VIA HSWAP)
MUST BE PULLED LOW DURING CONFIG
EXT SPI BOOT MODE (MASTER)

M2 (INT PULL UP VIA HSWAP)
MUST BE PULLED LOW DURING CONFIG
EXT SPI BOOT MODE (MASTER)

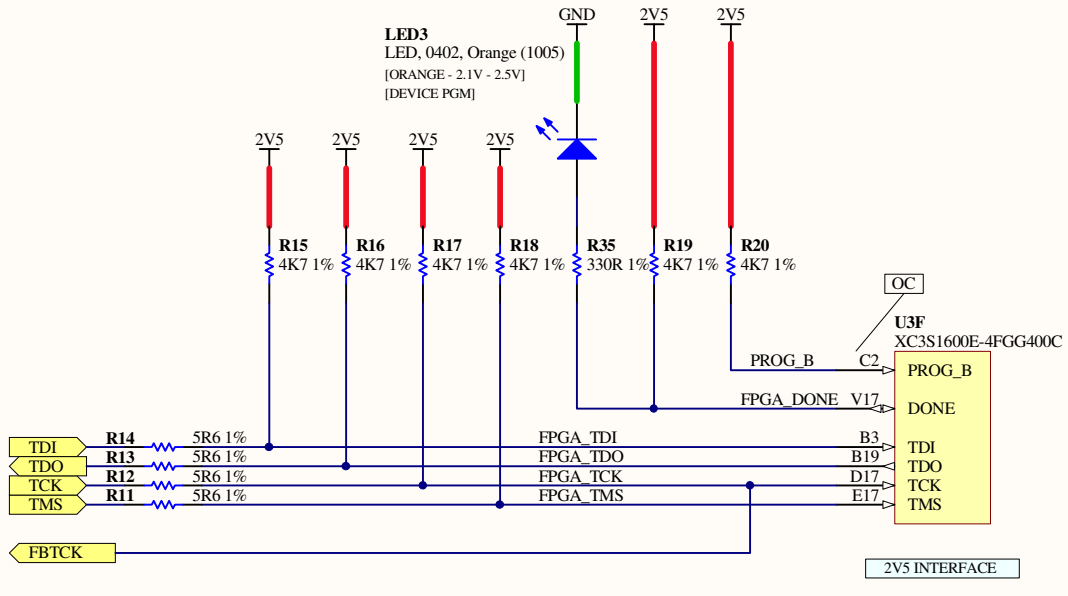
V20 SPI ACCESS SPEED (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
SPI SET TO FAST (000) (VCC0)

V51 SPI ACCESS SPEED (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
SPI SET TO FAST (000) (VCC0)

V52 SPI ACCESS SPEED (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
SPI SET TO FAST (000) (VCC0)



V20, V51, V52
V_SX = H
INTERNAL PULL UP BY HSWAP PRIOR TO CONFIG
V_S = FAST READ (000) (UG332-P99)

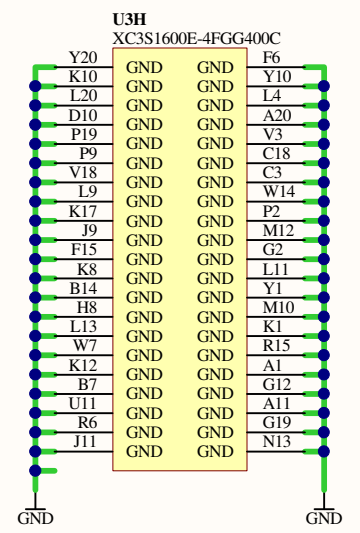
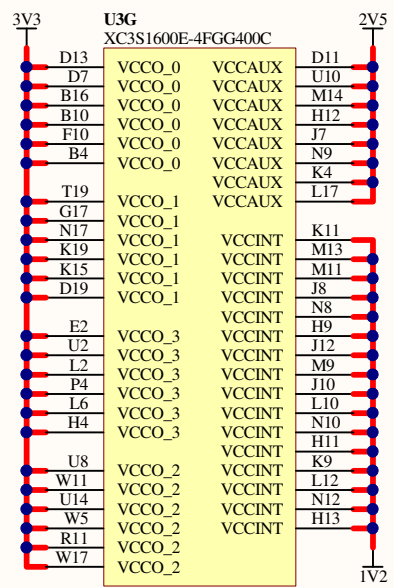


TDI, TDO, TCK AND TMS ALL REQUIRE SERIES RESISTOR FOR 3.3V OPERATION (XAPP453-P13)

FPGA_DONE PIN
H = PROGRAMMED (LOADED)
INTERNAL PULL UP
LOW BY DEFAULT

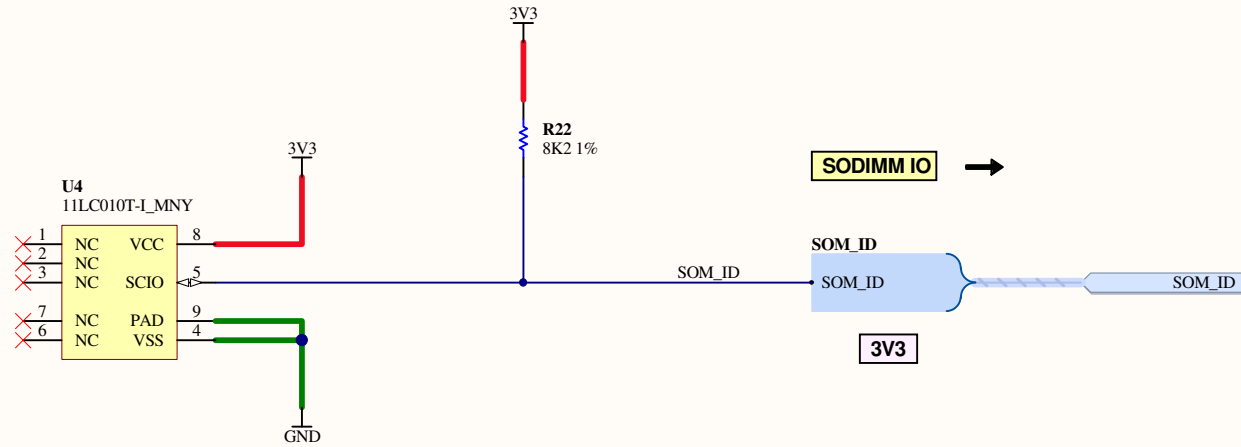
PROG_B (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
TO ALLOW CONFIGURATION TO START

DONE (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
HIGH = PROGRAM SUCCESSFUL

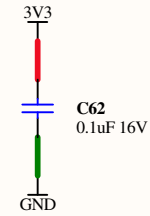


Sheet Title HOST FPGA Pwr and Programming			Altium Limited 3 Minna Close Belrose NSW 2085 Australia
Project Title SOM02			
Size: A4	Assy: TBA	Revision: 04	
Date: 23/09/2011	Time: 1:27:40 PM	Sheet 7 of 13	
File: FPGA_NonIO.SchDoc			

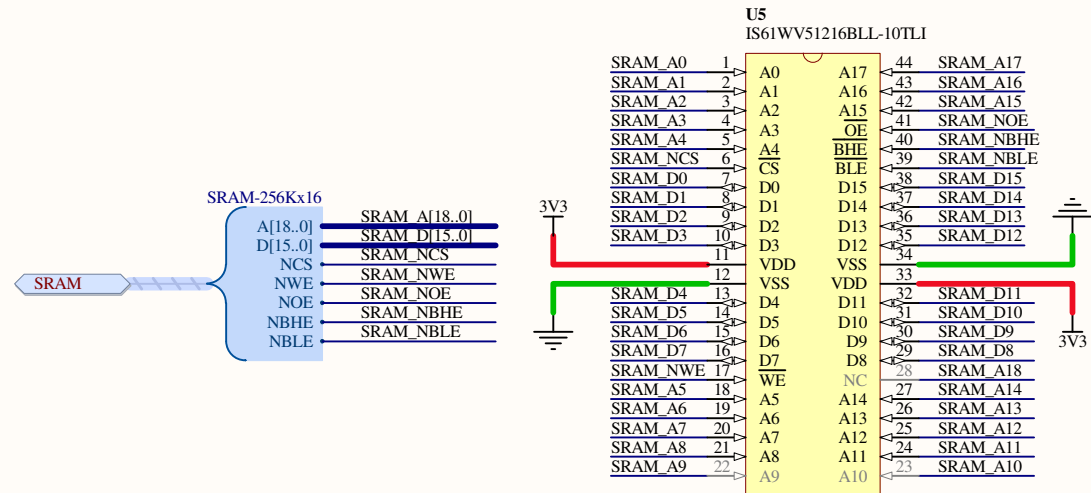




11LC010T-L_MNY POWER CONSUMPTION		
STANDBY:	3V3	1uA
ACTIVE:	3V3	1mA



Title		
Size A4	Number	Revision
Date:	23/09/2011	Sheet of
File:	CASRKH\SOM03 - XC3S1600E\SOM_ID_Schematic By:	



IS61WV25616BLS FAST SRAM (10nS)
 256K x16 BITS 512K bytes

DEFAULT
 IS61WV51216BLL-10TLI FAST SRAM (10nS)
 512K x16 BITS 1M bytes

IS61WV20488BLL-10TLI FAST SRAM (10nS)
 2048K x8 BITS 2M bytes



Sheet Title 256K x 16-Bit SRAM		Altium Limited 3 Minna Close Belrose NSW 2085 Australia		
Project Title SOM02				
Size: A4	Assy: TBA			Revision: 04
Date: 23/09/2011	Time: 1:27:40 PM			Sheet 9 of 0
File: SRAM_512Kx16_TSOP44.SchDoc				

1

2

3

4

A

A

B

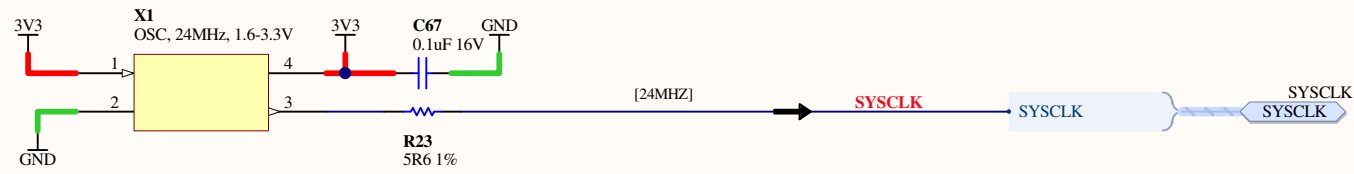
B


C

C

D

D



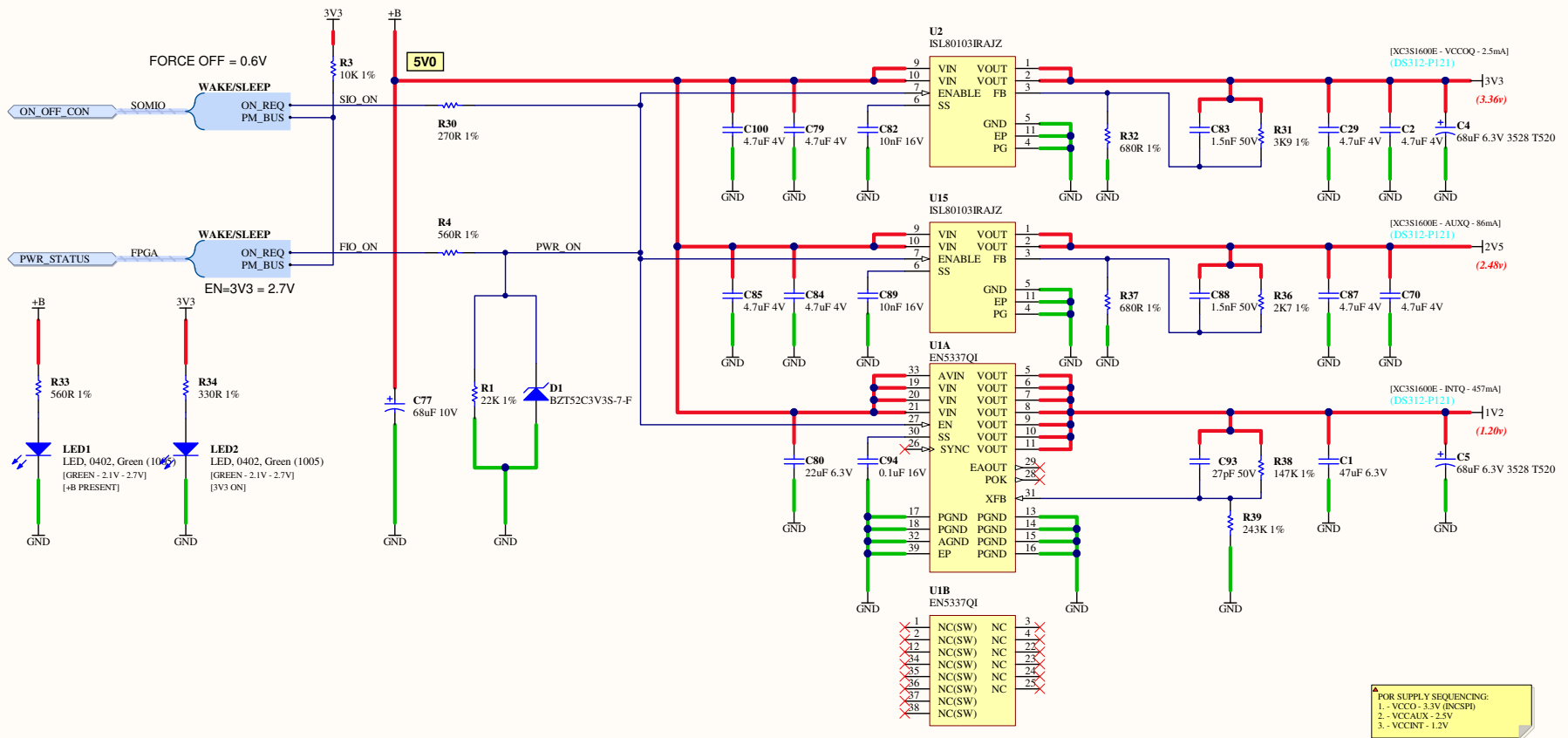
Sheet Title 16M x 32 SDRAM TSOP54 x 2		<i>Altium Limited</i> 3 Minna Close Belrose NSW 2085 Australia		
Project Title SOM02				
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Date: 23/09/2011	Time: 1:27:40 PM			Sheet 10 of 13
File: SYS_CLK.SchDoc				

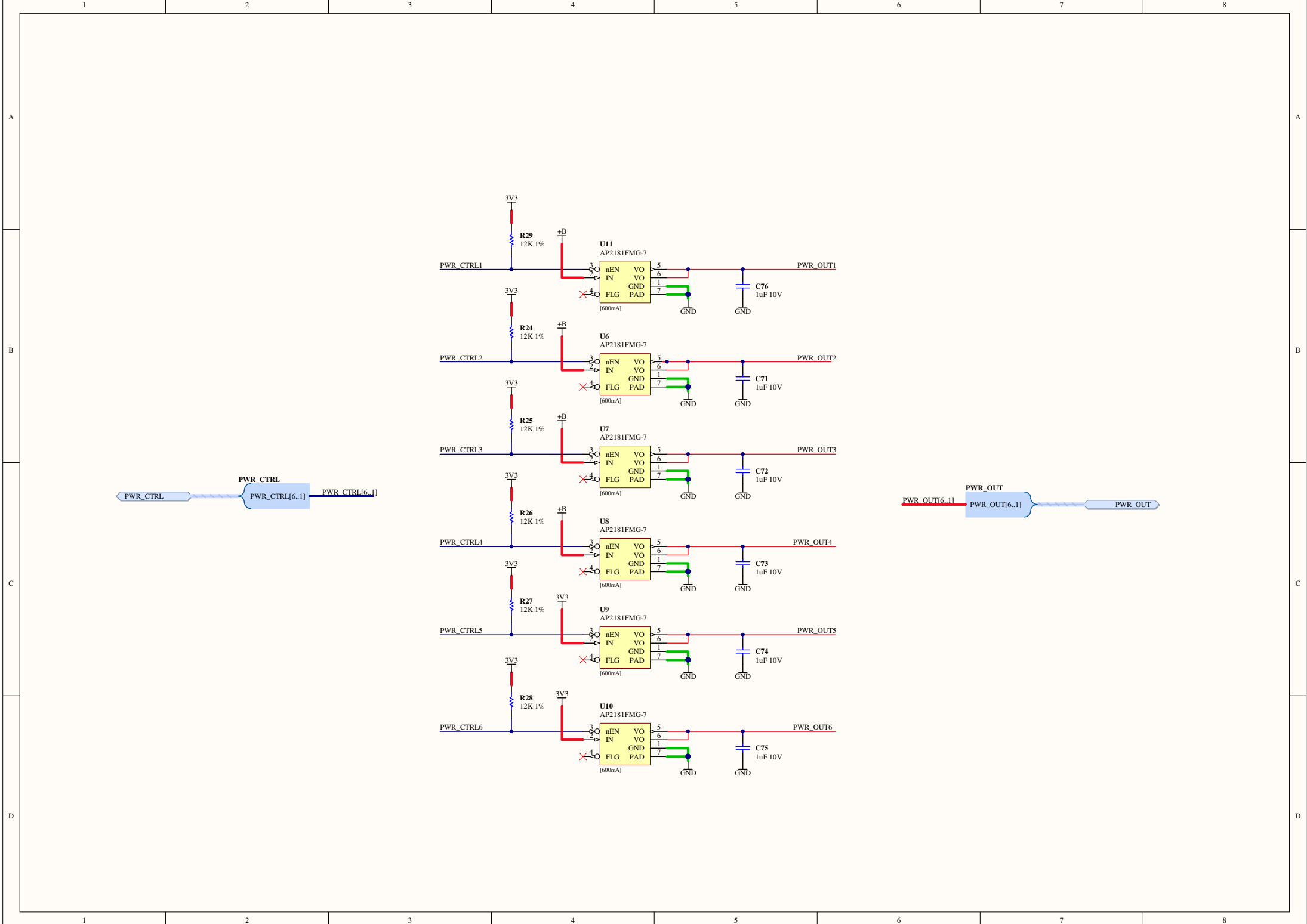
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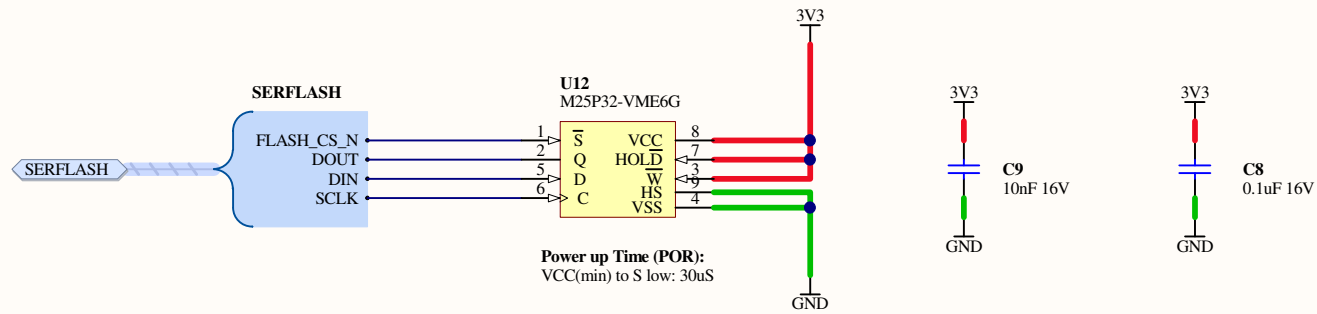
2

3

4







DEFAULT

M25P32-VME6G 32Mbit Serial PROM (75MHz)

33,554,432 BITS 4M bytes

(ID=0x2016)

M25P64-VME6G 64Mbit Serial PROM (75MHz)

67,108,864 BITS 8M bytes

(ID=0x2017)

M25P128-VME6G 128Mbit Serial PROM (54MHz)

134,217,728 BITS 16M bytes

(ID=0x2018)

W25Q256FV 256Mbit Serial PROM (80MHz)

268,435,456 BITS 32M bytes

(ID=0x4019)

Sheet Title *Host - Dual Serial Flash Memory*

Project Title *SOM02*

Size: A4

Assy: TBA

Revision: 04

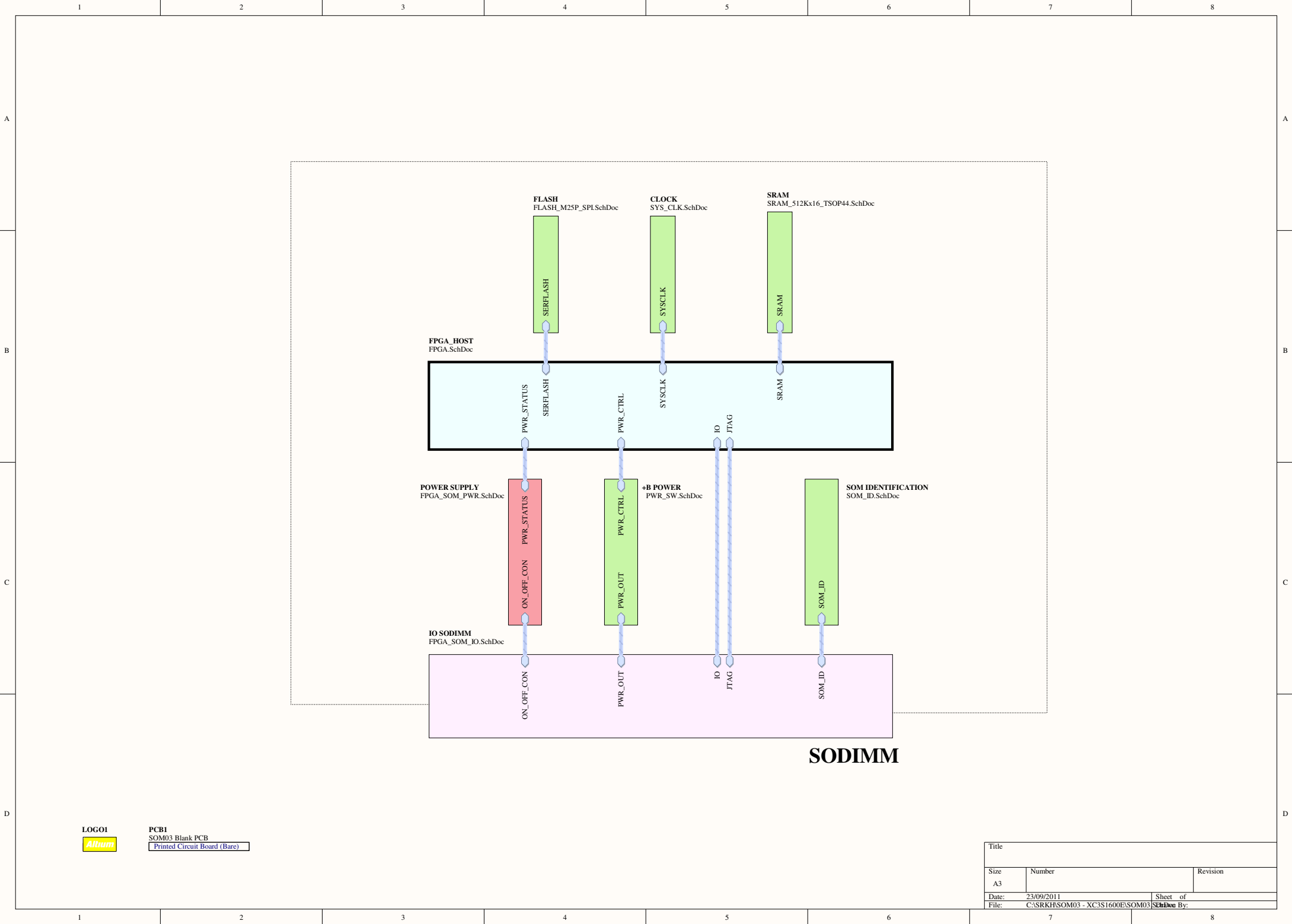
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Sheet 13 of 13

File: FLASH_M25P_SPI.SchDoc

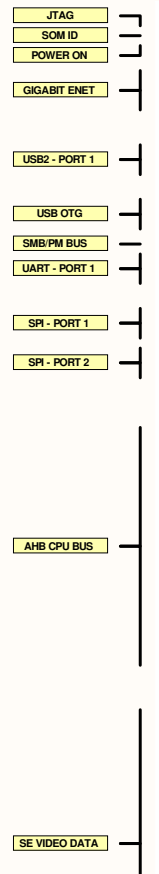
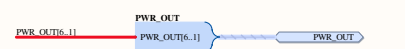
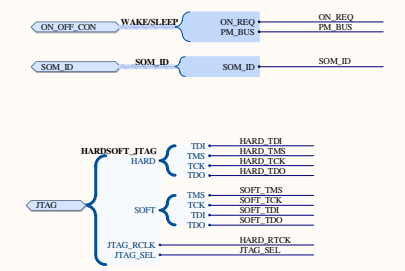
Altium Limited
3 Minna Close
Belrose
NSW 2085
Australia



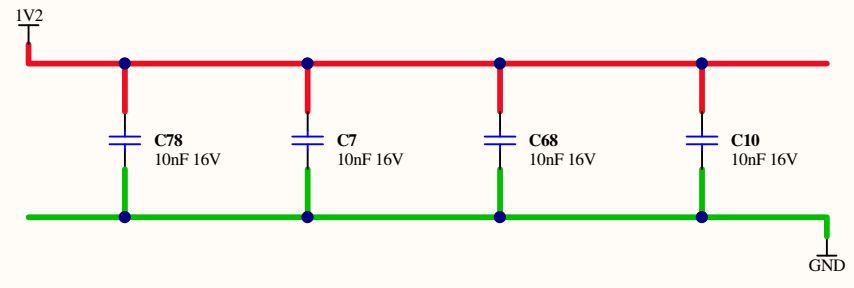
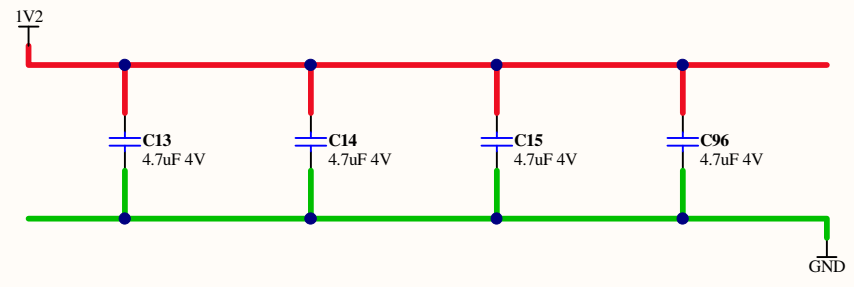
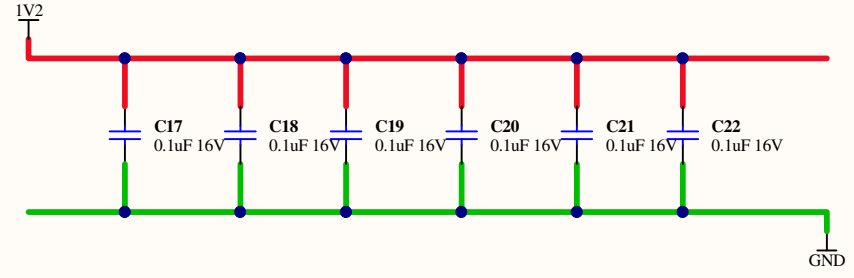



PCB1
SOM03 Blank PCB
Printed Circuit Board (Bare)

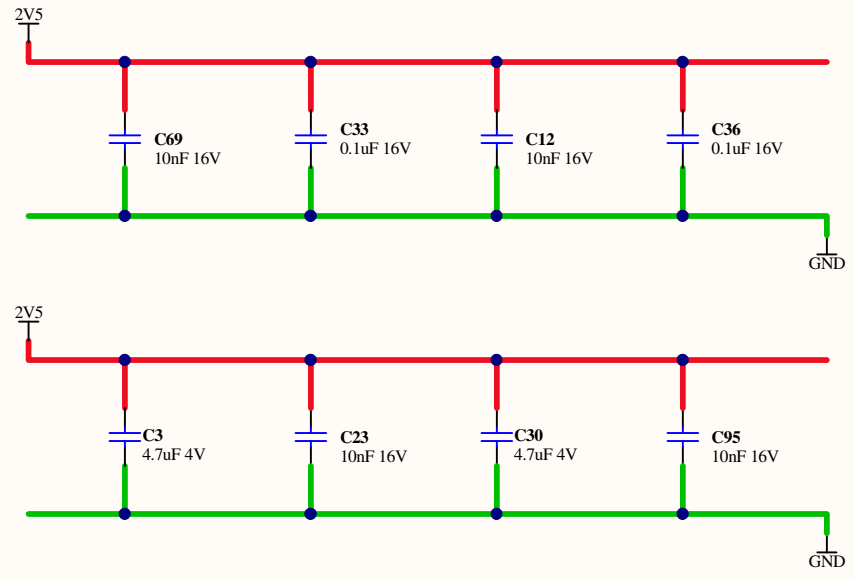
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A3		
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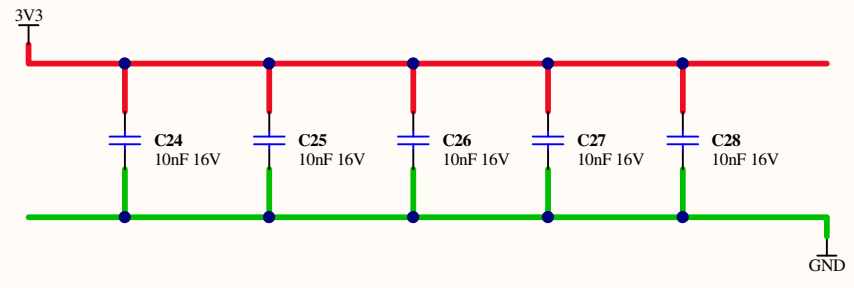
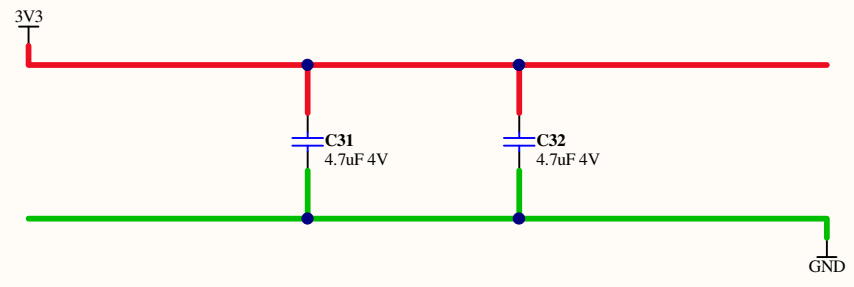
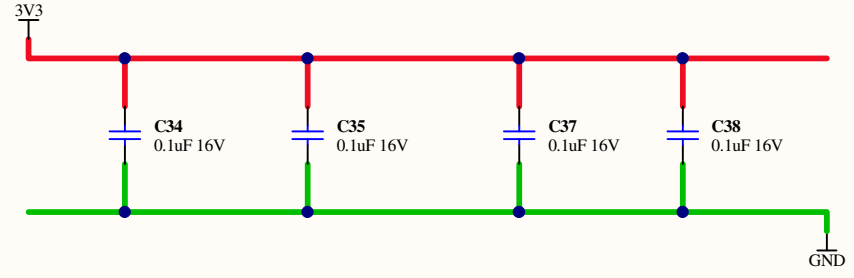
CNI			TOP			BOTTOM		
			COMP SIDE			SOLDER SIDE		
JTAG_TDI	HARD_TDI	1	JTAG_TDI	JTAG_TDI	2	HARD_TDO	JTAG_TDO	2
JTAG_TCK	HARD_TCK	4	JTAG_TCK	JTAG_TCK	5	HARD_TMS	JTAG_TMS	3
SOM_ID	ON_REQ	1	SOM_ID	ON_REQ	2	HARD_RCLK	JTAG_RCLK	3
ON_REQ	ON_REQ	2	MOD_WAKE	MOD_WAKE	7	JTAG_SEL	JTAG_SEL	4
ENET_Ap	GND	5	GND	GND	10	GND	GND	5
ENET_Ab	FPGA_I01	6	FPGA_I01	FPGA_I01	11	FPGA_I01	FPGA_I01	6
GND	FPGA_I02	7	FPGA_I02	FPGA_I02	12	FPGA_I02	FPGA_I02	7
ENET_Cp	GND	13	GND	GND	15	FPGA_I03	FPGA_I03	8
ENET_Cb	FPGA_I06	14	FPGA_I06	FPGA_I06	16	FPGA_I06	FPGA_I06	9
GND	GND	21	GND	GND	22	FPGA_I08	FPGA_I08	10
+B	GND	21	GND	GND	22	GND	GND	11
US2B_1_VBUS	PWR_OUT11	25	PWR_SW	PWR_SW	26	+B	+B	12
US2B_1_DP	PWR_OUT11	29	PWR_SW	PWR_SW	30	+B	+B	13
US2B_1_Dn	FPGA_I09	31	FPGA_I09	FPGA_I09	32	FPGA_I09	FPGA_I09	14
US2B2_DP	GND	37	GND	GND	38	GND	GND	15
US2B2_VBUS	FPGA_I03	39	FPGA_I03	FPGA_I03	40	US2B_2_VBUS	US2B_2_VBUS	16
US2B2_Dp	FPGA_I04	40	FPGA_I04	FPGA_I04	41	US2B2_Dp	US2B2_Dp	17
US2B2_Dn	FPGA_I05	41	FPGA_I05	FPGA_I05	42	GND	GND	18
US2B3_DP	GND	47	GND	GND	48	GND	GND	19
US2B3_Dp	FPGA_I07	49	FPGA_I07	FPGA_I07	50	US2B_3_VBUS	US2B_3_VBUS	20
US2B3_Dn	PWR_SW	51	PWR_SW	PWR_SW	52	US2B_3_VBUS	US2B_3_VBUS	21
US2BFG_VBUS	PWR_OUT13	53	PWR_SW	PWR_SW	54	US2B_3_VBUS	US2B_3_VBUS	22
US2BFG_DP	PWR_OUT13	57	PWR_SW	PWR_SW	58	US2B_3_VBUS	US2B_3_VBUS	23
US2BFG_Dn	FPGA_I015	59	FPGA_I015	FPGA_I015	60	US2B_3_VBUS	US2B_3_VBUS	24
US2BFG_VBUS	FPGA_I014	59	FPGA_I014	FPGA_I014	60	US2B_3_VBUS	US2B_3_VBUS	25
US2BFG_VBUS	PWR_OUT13	59	PWR_SW	PWR_SW	60	US2B_3_VBUS	US2B_3_VBUS	26
PM_BUS	PM_BUS	59	PM_BUS	PM_BUS	60	US2B_3_VBUS	US2B_3_VBUS	27
UART1_TXD	SOFT_TDO	59	SOFT_TDO	SOFT_TDO	60	US2B_3_VBUS	US2B_3_VBUS	28
UART1_RTS	SOFT_TMS	59	SOFT_TMS	SOFT_TMS	60	US2B_3_VBUS	US2B_3_VBUS	29
UART1_RXD	SOFT_TCK	59	SOFT_TCK	SOFT_TCK	60	US2B_3_VBUS	US2B_3_VBUS	30
UART1_CTS	SOFT_TDI	59	SOFT_TDI	SOFT_TDI	60	US2B_3_VBUS	US2B_3_VBUS	31
GND	SOFT_TCK	59	SOFT_TCK	SOFT_TCK	60	US2B_3_VBUS	US2B_3_VBUS	32
SPI1_TXD	GND	59	GND	GND	60	US2B_3_VBUS	US2B_3_VBUS	33
SPI1_RXD	FPGA_I021	59	FPGA_I021	FPGA_I021	60	US2B_3_VBUS	US2B_3_VBUS	34
SPI1_CLK	FPGA_I025	59	FPGA_I025	FPGA_I025	60	US2B_3_VBUS	US2B_3_VBUS	35
SPI1_CS	FPGA_I026	59	FPGA_I026	FPGA_I026	60	US2B_3_VBUS	US2B_3_VBUS	36
SPI2_TXD	FPGA_I027	59	FPGA_I027	FPGA_I027	60	US2B_3_VBUS	US2B_3_VBUS	37
SPI2_RXD	FPGA_I032	59	FPGA_I032	FPGA_I032	60	US2B_3_VBUS	US2B_3_VBUS	38
SPI2_CLK	FPGA_I033	59	FPGA_I033	FPGA_I033	60	US2B_3_VBUS	US2B_3_VBUS	39
SPI2_CS	FPGA_I034	59	FPGA_I034	FPGA_I034	60	US2B_3_VBUS	US2B_3_VBUS	40
GND	FPGA_I035	59	FPGA_I035	FPGA_I035	60	US2B_3_VBUS	US2B_3_VBUS	41
+B	GND	77	GND	GND	78	US2B_3_VBUS	US2B_3_VBUS	42
+B	GND	77	GND	GND	78	US2B_3_VBUS	US2B_3_VBUS	43
+B	GND	77	GND	GND	78	US2B_3_VBUS	US2B_3_VBUS	44
+B	GND	77	GND	GND	78	US2B_3_VBUS	US2B_3_VBUS	45
BUS_A0	FPGA_I040	83	FPGA_I040	FPGA_I040	84	BUS_D0	BUS_D0	46
BUS_A1	FPGA_I041	84	FPGA_I041	FPGA_I041	85	BUS_D1	BUS_D1	47
BUS_A2	FPGA_I042	85	FPGA_I042	FPGA_I042	86	BUS_D2	BUS_D2	48
BUS_A3	FPGA_I043	86	FPGA_I043	FPGA_I043	87	BUS_D3	BUS_D3	49
BUS_A4	FPGA_I044	87	FPGA_I044	FPGA_I044	88	BUS_D4	BUS_D4	50
BUS_A5	FPGA_I045	88	FPGA_I045	FPGA_I045	89	BUS_D5	BUS_D5	51
BUS_A6	FPGA_I046	89	FPGA_I046	FPGA_I046	90	BUS_D6	BUS_D6	52
BUS_A7	FPGA_I047	90	FPGA_I047	FPGA_I047	91	BUS_D7	BUS_D7	53
+B	FPGA_I047	90	FPGA_I047	FPGA_I047	91	BUS_D8	BUS_D8	54
BUS_A8	GND	91	GND	GND	92	BUS_D9	BUS_D9	55
BUS_A9	FPGA_I048	91	FPGA_I048	FPGA_I048	92	BUS_D9	BUS_D9	56
BUS_A10	FPGA_I049	92	FPGA_I049	FPGA_I049	93	BUS_D10	BUS_D10	57
BUS_A11	FPGA_I050	93	FPGA_I050	FPGA_I050	94	BUS_D11	BUS_D11	58
BUS_A12	FPGA_I051	94	FPGA_I051	FPGA_I051	95	BUS_D12	BUS_D12	59
BUS_A13	FPGA_I052	95	FPGA_I052	FPGA_I052	96	BUS_D13	BUS_D13	60
BUS_A14	FPGA_I053	96	FPGA_I053	FPGA_I053	97	BUS_D14	BUS_D14	61
BUS_A15	FPGA_I054	97	FPGA_I054	FPGA_I054	98	BUS_D15	BUS_D15	62
GND	FPGA_I055	98	FPGA_I055	FPGA_I055	99	GND	GND	63
BUS_A16	GND	117	GND	GND	118	BUS_CSD	BUS_CSD	64
BUS_A17	FPGA_I056	118	FPGA_I056	FPGA_I056	119	BUS_CSD	BUS_CSD	65
BUS_A18	FPGA_I057	119	FPGA_I057	FPGA_I057	120	BUS_CSD	BUS_CSD	66
BUS_A19	FPGA_I058	120	FPGA_I058	FPGA_I058	121	BUS_CSD	BUS_CSD	67
BUS_A20	FPGA_I059	121	FPGA_I059	FPGA_I059	122	BUS_CSD	BUS_CSD	68
BUS_DMACK	FPGA_I060	122	FPGA_I060	FPGA_I060	123	BUS_CSD	BUS_CSD	69
BUS_DMARQ	FPGA_I061	123	FPGA_I061	FPGA_I061	124	BUS_CSD	BUS_CSD	70
BUS_A10V	FPGA_I062	124	FPGA_I062	FPGA_I062	125	BUS_CSD	BUS_CSD	71
BUS_A0E	FPGA_I063	125	FPGA_I063	FPGA_I063	126	BUS_CSD	BUS_CSD	72
+B	FPGA_I064	126	FPGA_I064	FPGA_I064	127	BUS_CSD	BUS_CSD	73
+B	FPGA_I064	126	FPGA_I064	FPGA_I064	127	BUS_CSD	BUS_CSD	74
+B	FPGA_I064	126	FPGA_I064	FPGA_I064	127	BUS_CSD	BUS_CSD	75
+B	FPGA_I064	126	FPGA_I064	FPGA_I064	127	BUS_CSD	BUS_CSD	76
FXD0[ANK]	FPGA_I066	127	FPGA_I066	FPGA_I066	128	SD1_DAT0	SD1_DAT0	77
FXD0[0]	FPGA_I068	128	FPGA_I068	FPGA_I068	129	SD1_DAT1	SD1_DAT1	78
FXD0[1]	FPGA_I069	129	FPGA_I069	FPGA_I069	130	SD1_DAT2	SD1_DAT2	79
FXD0[2]	FPGA_I070	130	FPGA_I070	FPGA_I070	131	SD1_DAT3	SD1_DAT3	80
FXD0[3]	FPGA_I071	131	FPGA_I071	FPGA_I071	132	SD1_CMD	SD1_CMD	81
FXD0[4]	FPGA_I072	132	FPGA_I072	FPGA_I072	133	SD1_CLK	SD1_CLK	82
FXD0[5]	FPGA_I073	133	FPGA_I073	FPGA_I073	134	SD1_CD	SD1_CD	83
FXD0[6]	FPGA_I074	134	FPGA_I074	FPGA_I074	135	SD1_PWR	SD1_PWR	84
FXD0[7]	FPGA_I075	135	FPGA_I075	FPGA_I075	136	SD2_DAT0	SD2_DAT0	85
FXD0[8]	FPGA_I076	136	FPGA_I076	FPGA_I076	137	SD2_DAT1	SD2_DAT1	86
FXD0[9]	FPGA_I077	137	FPGA_I077	FPGA_I077	138	SD2_DAT2	SD2_DAT2	87
FXD0[10]	FPGA_I078	138	FPGA_I078	FPGA_I078	139	SD2_DAT3	SD2_DAT3	88
FXD0[11]	FPGA_I079	139	FPGA_I079	FPGA_I079	140	SD2_CMD	SD2_CMD	89
FXD0[12]	FPGA_I080	140	FPGA_I080	FPGA_I080	141	SD2_CLK	SD2_CLK	90
FXD0[13]	FPGA_I081	141	FPGA_I081	FPGA_I081	142	SD2_CD	SD2_CD	91
FXD0[14]	FPGA_I082	142	FPGA_I082	FPGA_I082	143	SD2_PWR	SD2_PWR	92
FXD0[15]	FPGA_I083	143	FPGA_I083	FPGA_I083	144	DPDVI_HPD	DPDVI_HPD	93
FXD0[16]	FPGA_I084	144	FPGA_I084	FPGA_I084	145	DPDVI_CLK	DPDVI_CLK	94
FXD0[17]	FPGA_I085	145	FPGA_I085	FPGA_I085	146	DPDVI_n0	DPDVI_n0	95
FXD0[18]	FPGA_I086	146	FPGA_I086	FPGA_I086	147	DPDVI_n1	DPDVI_n1	96
FXD0[19]	FPGA_I087	147	FPGA_I087	FPGA_I087	148	DPDVI_n2	DPDVI_n2	97
FXD0[20]	FPGA_I088	148	FPGA_I088	FPGA_I088	149	DPDVI_n3	DPDVI_n3	98
FXD0[21]	FPGA_I089	149	FPGA_I089	FPGA_I089	150	DPDVI_n4	DPDVI_n4	99
FXD0[22]	FPGA_I090	150	FPGA_I090	FPGA_I090	151	DPDVI_n5	DPDVI_n5	100
FXD0[23]	FPGA_I091	151	FPGA_I091	FPGA_I091	152	DPDVI_n6	DPDVI_n6	101
FXD0[24]	FPGA_I092	152	FPGA_I092	FPGA_I092	153	DPDVI_n7	DPDVI_n7	102
FXD0[25]	FPGA_I093	153	FPGA_I093	FPGA_I093	154	DPDVI_n8	DPDVI_n8	103
FXD0[26]	FPGA_I094	154	FPGA_I094	FPGA_I094	155	DPDVI_n9	DPDVI_n9	104
FXD0[27]	FPGA_I095	155	FPGA_I095	FPGA_I095	156	DPDVI_n10	DPDVI_n10	105
FXD0[28]	FPGA_I096	156	FPGA_I096	FPGA_I096	157	DPDVI_n11	DPDVI_n11	106
FXD0[29]	FPGA_I097	157	FPGA_I097	FPGA_I097	158	DPDVI_n12	DPDVI_n12	107
FXD0[30]	FPGA_I098	158	FPGA_I098	FPGA_I098	159	DPDVI_n13	DPDVI_n13	108
FXD0[31]	FPGA_I099	159	FPGA_I099	FPGA_I099	160	DPDVI_n14	DPDVI_n14	109
FXD0[32]	FPGA_I100	160	FPGA_I100	FPGA_I100	161	DPDVI_n15	DPDVI_n15	110
FXD0[33]	FPGA_I101	161	FPGA_I101	FPGA_I101	162	DPDVI_n16	DPDVI_n16	111
FXD0[34]	FPGA_I102	162	FPGA_I102	FPGA_I102	163	DPDVI_n17	DPDVI_n17	112
FXD0[35]	FPGA_I103	163	FPGA_I103	FPGA_I103	164	DPDVI_n18	DPDVI_n18	113
FXD0[36]	FPGA_I104	164	FPGA_I104	FPGA_I104	165	DPDVI_n19	DPDVI_n19	114
FXD0[37]	FPGA_I105	165	FPGA_I105	FPGA_I105	166	DPDVI_n20	DPDVI_n20	115
FXD0[38]	FPGA_I106	166	FPGA_I106	FPGA_I106	167	DPDVI_n21	DPDVI_n21	116
FXD0[39]	FPGA_I107	167	FPGA_I107	FPGA_I107	168	DPDVI_n22	DPDVI_n22	117
FXD0[40]	FPGA_I108	168	FPGA_I108	FPGA_I108	169	DPDVI_n23	DPDVI_n23	118
FXD0[41]	FPGA_I109	169	FPGA_I109	FPGA_I109	170	DPDVI_n24	DPDVI_n24	119
FXD0[42]	FPGA_I110	170	FPGA_I110	FPGA_I110	171	DPDVI_n25	DPDVI_n25	120
FXD0[43]	FPGA_I111	171	FPGA_I111	FPGA_I111	172	DPDVI_n26	DPDVI_n26	121
FXD0[44]	FPGA_I112	172	FPGA_I112	FPGA_I112	173	DPDVI_n27	DPDVI_n27	122
FXD0[45]	FPGA_I113	173	FPGA_I113	FPGA_I113	174	DPDVI_n28	DPDVI_n28	123
FXD0[46]	FPGA_I114	174	FPGA_I114	FPGA_I114	175	DPDVI_n29	DPDVI_n29	124
FXD0[47]	FPGA_I115	175	FPGA_I115	FPGA_I115	176	DPDVI_n30	DPDVI_n30	125
FXD0[48]	GND	176	GND	GND	177	DPDVI_n31	DPDVI_n31	126
FXD0[49]	GND	177	GND	GND	178	DPDVI_n32	DPDVI_n32	127
FXD0[50]	GND	178	GND	GND	179	DPDVI_n33	DPDVI_n33	128
FXD0[51]	GND	179	GND	GND	180	DPDVI_n34	DPDVI_n34	129
FXD0[52]	GND	180	GND	GND	181	DPDVI_n35	DPDVI_n35	130
FXD0[53]	GND	181	GND	GND	182	DPDVI_n36	DPDVI_n36	131
FXD0[54]	GND	182	GND	GND	183	DPDVI_n37	DPDVI_n37	132
FXD0[55]	GND	183	GND	GND	184	DPDVI_n38	DPDVI_n38	133
FXD0[56]	GND	184	GND	GND	185	DPDVI_n39	DPDVI_n39	134
FXD0[57]	GND	185	GND	GND	186	DPDVI_n40	DPDVI_n40	135
FXD0[58]	GND	186	GND	GND	187	DPDVI_n41	DPDVI_n41	136
FXD0[59]	GND	187	GND	GND	188	DPDVI_n42	DPDVI_n42	137
FXD0[60]	GND	188	GND	GND	189	DPDVI_n43	DPDVI_n43	138
FXD0[61]	GND	189	GND	GND	190	DPDVI_n44	DPDVI_n44	139
FXD0[62]	GND	190	GND	GND	191	DPDVI_n45	DPDVI_n45	140
FXD0[63]	GND	191	G					




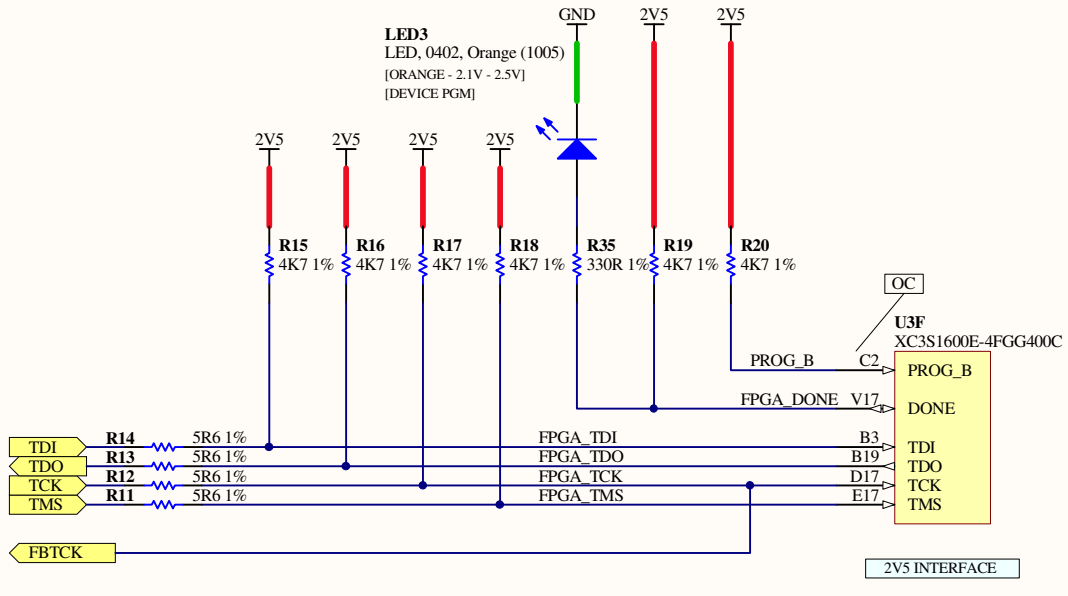
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Project Title SOM02			
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Date: 23/09/2011	Time: 1:27:40 PM	Sheet 3 of 13	
File: FPGA_Bypass_FPGA_1V2.SchDoc			



Sheet Title FPGA Bypass 2V5		<i>Altium Limited</i> 3 Minna Close Belrose NSW 2085 Australia		
Project Title SOM02				
Size: A4	Assy: TBA			Revision: 04
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Sheet Title FPGA Bypass 2V5		Altium Limited 3 Minna Close Belrose NSW 2085 Australia	
Project Title SOM02			
Size: A4	Assy: TBA	Revision: 04	
Date: 23/09/2011	Time: 1:27:40 PM	Sheet 5 of 13	
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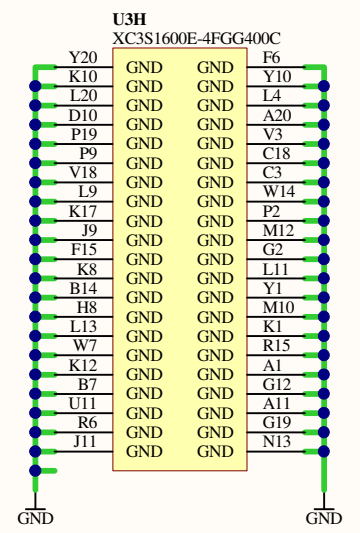
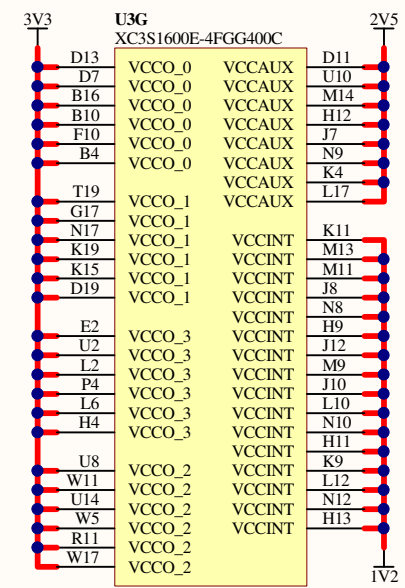


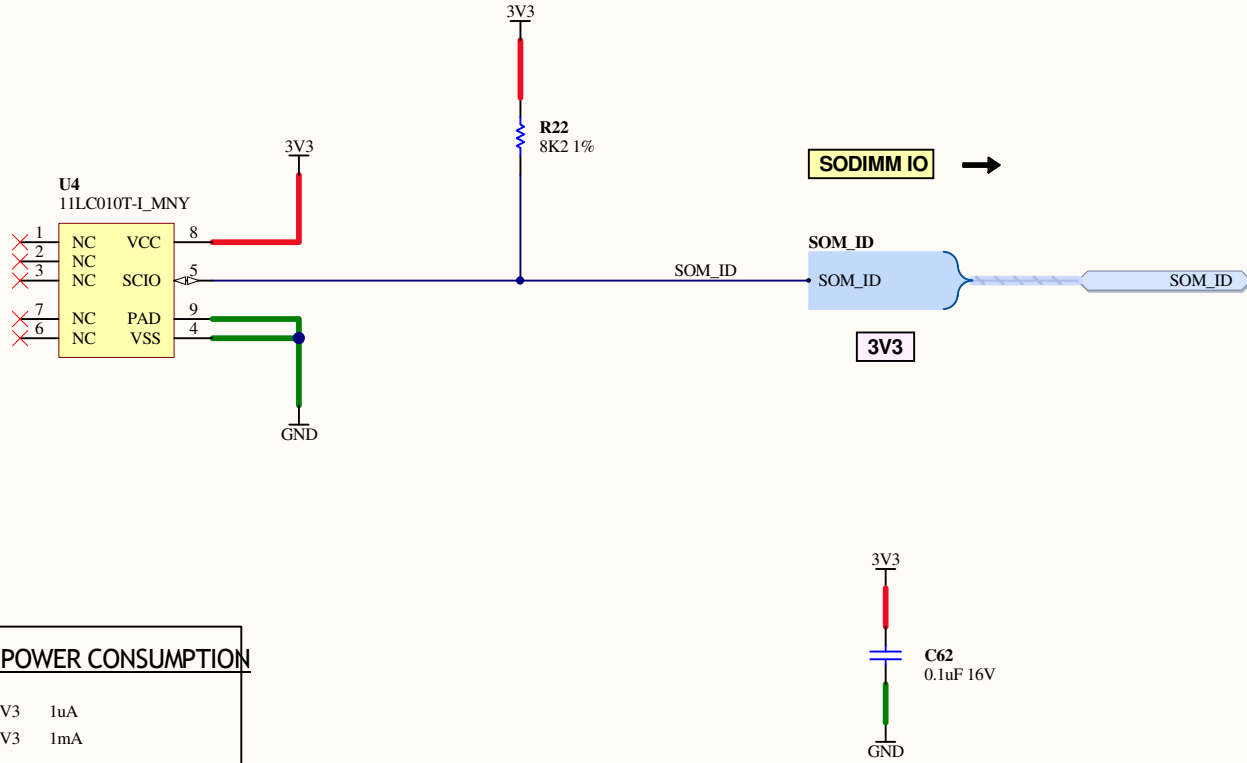
TDI, TDO, TCK AND TMS ALL REQUIRE SERIES RESISTOR FOR 3.3V OPERATION (XAPP453-P13)

FPGA_DONE PIN
H = PROGRAMMED (LOADED)
INTERNAL PULL UP
LOW BY DEFAULT

PROG_B (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
TO ALLOW CONFIGURATION TO START

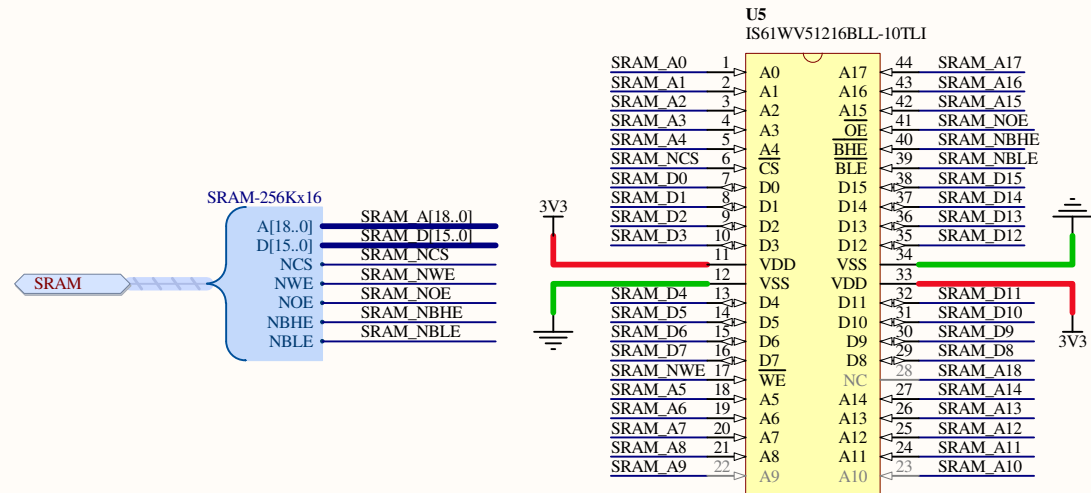
DONE (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
HIGH = PROGRAM SUCCESSFUL





11LC010T-L_MNY POWER CONSUMPTION		
STANDBY:	3V3	1uA
ACTIVE:	3V3	1mA

Title		
Size A4	Number	Revision
Date:	23/09/2011	Sheet of
File:	CASRKH\SOM03 - XC3S1600E\SOM_ID_Schematic By:	



IS61WV25616BLS FAST SRAM (10nS)
 256K x16 BITS 512K bytes

DEFAULT
 IS61WV51216BLL-10TLI FAST SRAM (10nS)
 512K x16 BITS 1M bytes

IS61WV20488BLL-10TLI FAST SRAM (10nS)
 2048K x8 BITS 2M bytes



Sheet Title 256K x 16-Bit SRAM		Altium Limited 3 Minna Close Belrose NSW 2085 Australia		
Project Title SOM02				
Size: A4	Assy: TBA			Revision: 04
Date: 23/09/2011	Time: 1:27:40 PM			Sheet 9 of 0
File: SRAM_512Kx16_TSOP44.SchDoc				

1

2

3

4

A

A

B

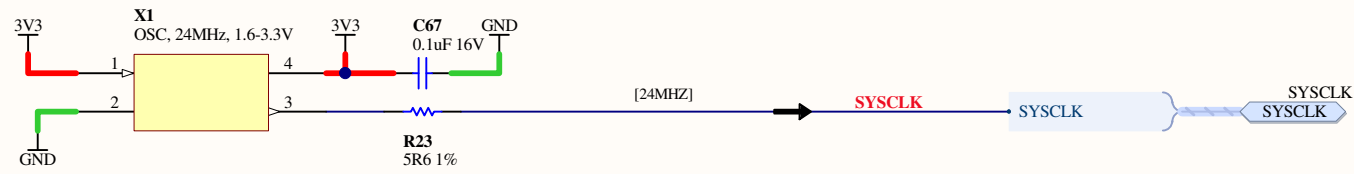
B


C

C

D

D



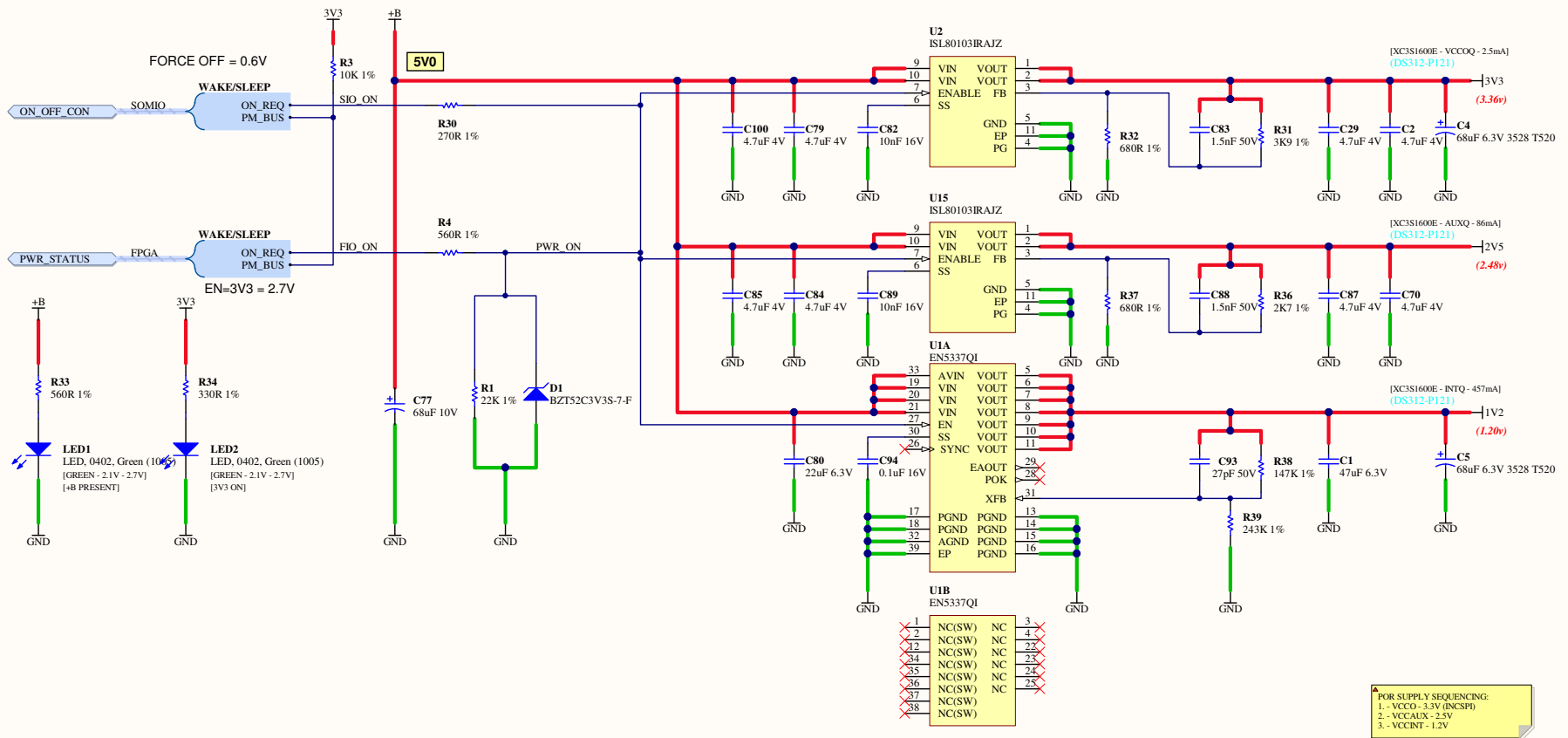
Sheet Title 16M x 32 SDRAM TSOP54 x 2		<i>Altium Limited</i> 3 Minna Close Belrose NSW 2085 Australia		
Project Title SOM02				
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Date: 23/09/2011	Time: 1:27:40 PM			Sheet 10 of 13
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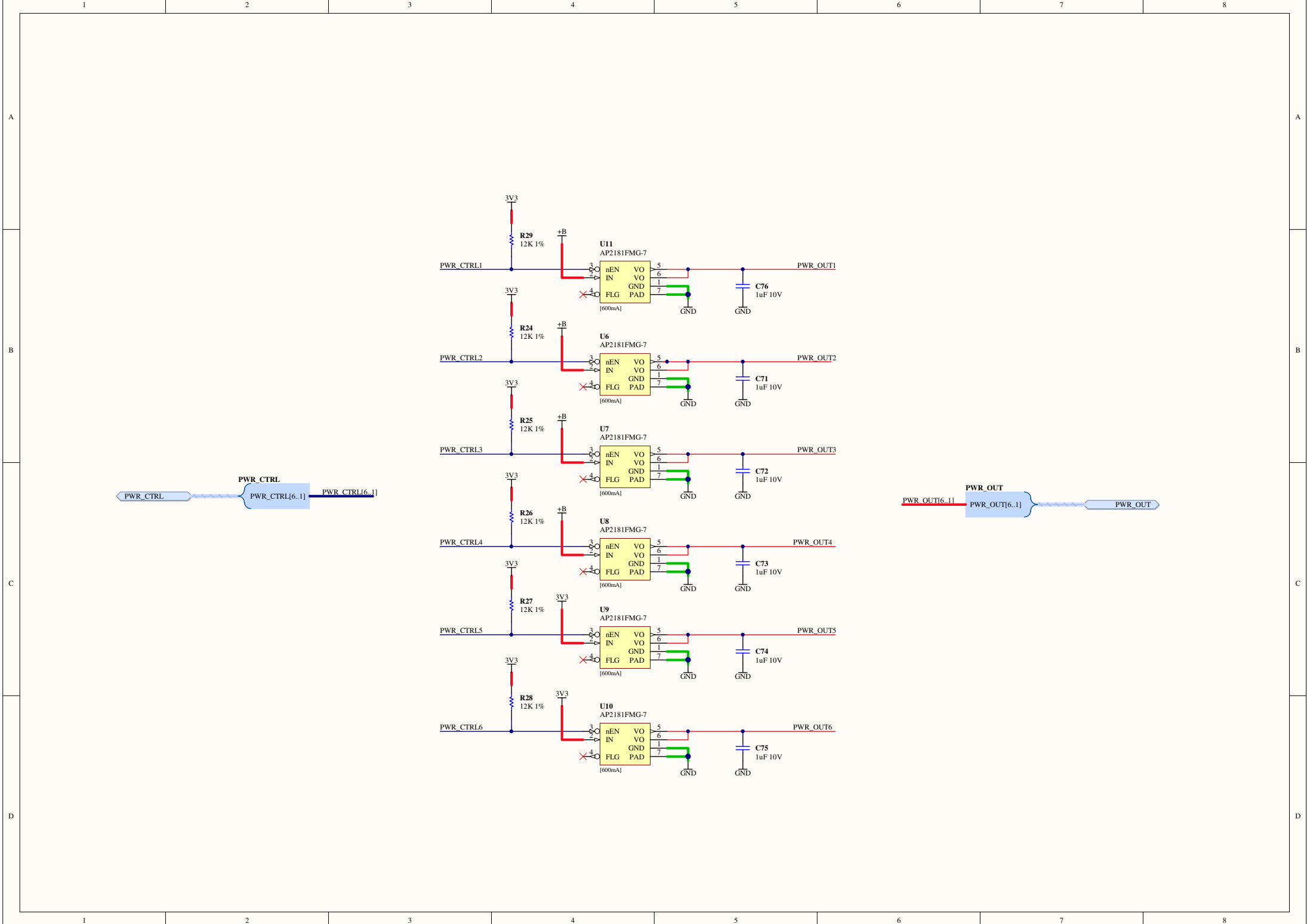
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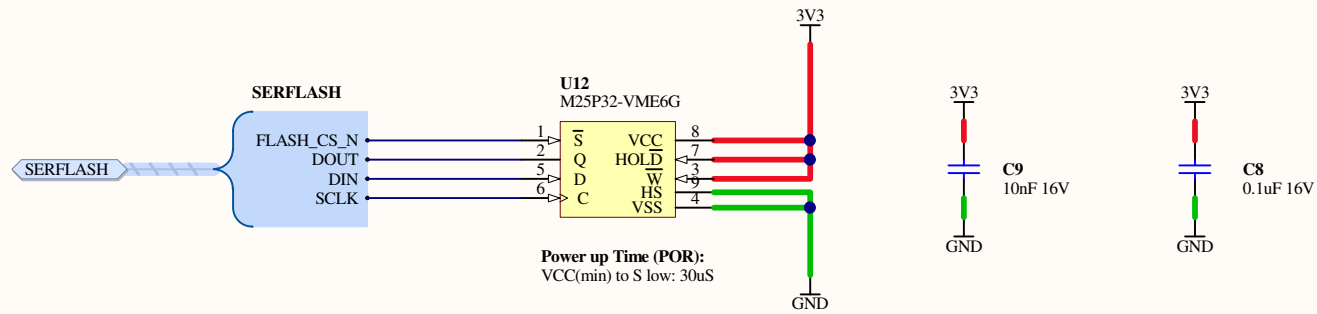
3

4



A
POR SUPPLY SEQUENCING:
 1. - VCCO - 3.3V (MCSPI)
 2. - VCCAUX - 2.5V
 3. - VCCINT - 1.2V





DEFAULT

M25P32-VME6G 32Mbit Serial PROM (75MHz)

33,554,432 BITS 4M bytes

(ID=0x2016)

M25P64-VME6G 64Mbit Serial PROM (75MHz)

67,108,864 BITS 8M bytes

(ID=0x2017)

M25P128-VME6G 128Mbit Serial PROM (54MHz)

134,217,728 BITS 16M bytes

(ID=0x2018)

W25Q256FV 256Mbit Serial PROM (80MHz)

268,435,456 BITS 32M bytes

(ID=0x4019)

Sheet Title *Host - Dual Serial Flash Memory*

Project Title *SOM02*

Size: A4

Assy: TBA

Revision: 04

Date: 23/09/2011 Time: 1:27:40 PM

Sheet 13 of 13

File: FLASH_M25P_SPI.SchDoc

Altium Limited
3 Minna Close
Belrose
NSW 2085
Australia

