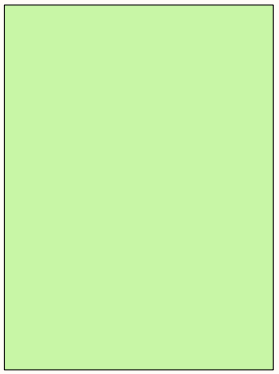
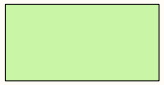
U_DB_Common
DB_Common.SchDoc



U_PSU
PSU.SCHDOC

U_Bypass_Board
DB_Bypass.SchDoc



U_TB11_Hardware_Kit
TB11_Hardware_Kit.SchDoc

Sheet Title	***TB11 - Top Level Schematic***		
Project Title	***TB11 Nanoconnector Test Jig***		
Size: A4	Assy: D-820-0034	Revision: 01	
Date: 9/24/2011	Time: 12:00:42 AM	Sheet 1 of 16	
File: TB11_Top.SchDoc			

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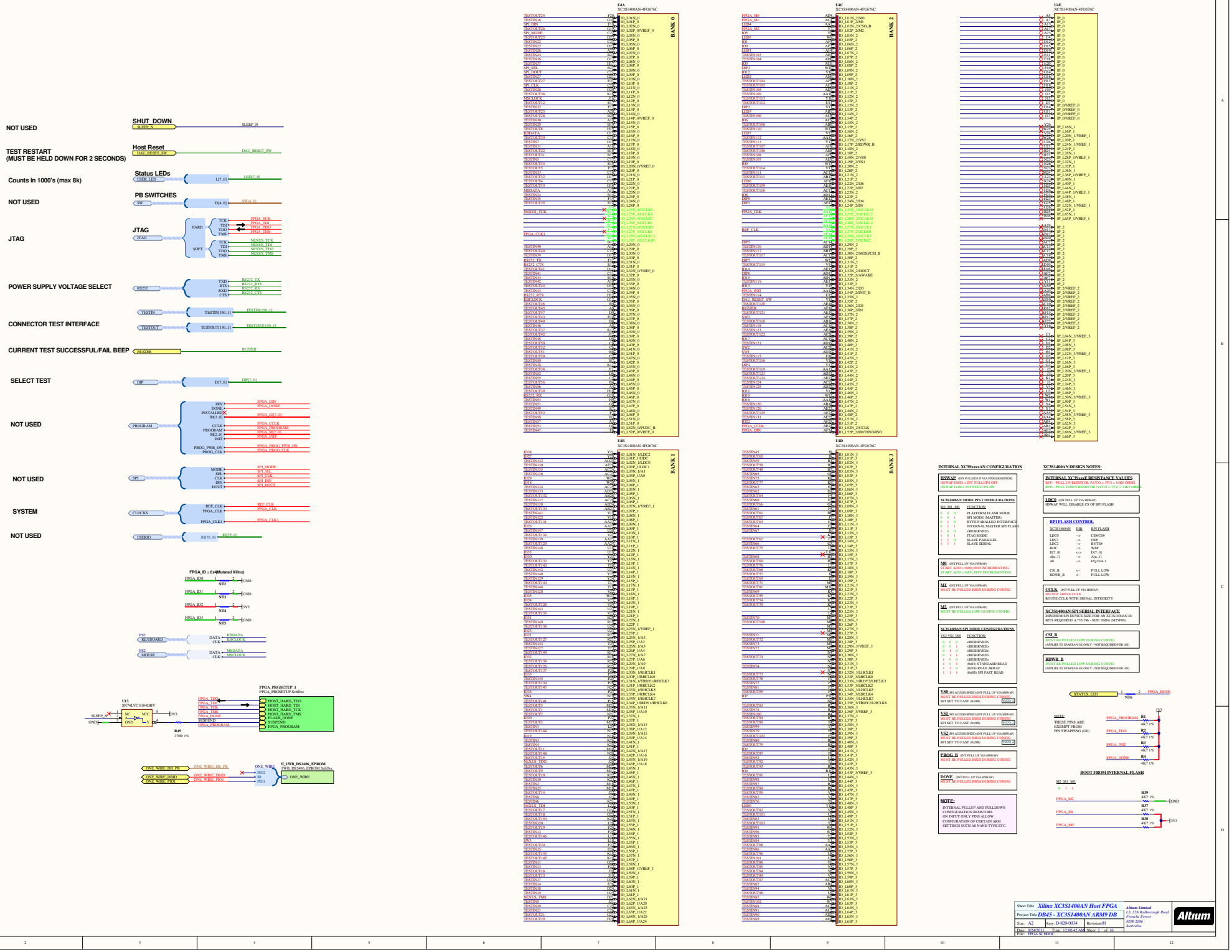
NOT USED
SHUT_DOWN
SLEEP_N
TEST RESTART
(MUST BE HELD DOWN FOR 2 SECONDS)
Host Reset
DAU_RESET_SW
Counts in 1000's (max 8k)
Status LEDs
USER_LED
LED[7..0]
NOT USED
PB SWITCHES
SW
SW[4..0]
JTAG
JTAG
HARD
SOFT
TCK
TDI
TDO
TMS
FPGA_TCK
FPGA_TDI
FPGA_TDO
FPGA_TMS
NEXUS_TCK
NEXUS_TDI
NEXUS_TDO
NEXUS_TMS
POWER SUPPLY VOLTAGE SELECT
RS232
TXD
RTS
RXD
CTS
RS232_TX
RS232_RTS
RS232_RX
RS232_CTS
CONNECTOR TEST INTERFACE
TESTIN
TESTIN[150..1]
TESTOUT
TESTOUT[150..1]
CURRENT TEST SUCCESSFUL/FAIL BEEP
BUZZER
SELECT TEST
DIP
DIP[7..0]
NOT USED
PROGRAM
DIN
DONE
INSTALLED
ID[3..0]
CCLK
PROGRAM
M2..0]
INIT
PROG_PWR_ON
PROG_CLK
FPGA_DIN
FPGA_DONE
FPGA_ID[3..0]
FPGA_CCLK
FPGA_PROGRAM
FPGA_M[2..0]
FPGA_INIT
FPGA_PROG_PWR_ON
FPGA_PROG_CLK
NOT USED
SPI
MODE
SEL
CLK
DIN
DOUT
SPI_MODE
SPI_SEL
SPI_CLK
SPI_DIN
SPI_DOUT
SYSTEM
CLOCKS
REF_CLK
FPGA_CLK
FPGA_CLK1
NOT USED
USERID
IO[35..0]
FPGA_ID = 0x4(Mutated Xilinx)
FPGA_ID0
FPGA_ID1
FPGA_ID2
FPGA_ID3
NT2
NT3
NT4
NT5
GND
3V3
PS2
KEYBOARD
MOUSE
DATA
CLK
KBDATA
KBCLOCK
MSDATA
MSCLOCK
U13
SN74LVC1G04DBV
SLEEP_N
3V3
R45
270R 1%
FPGA_PRGSETUP_1
FPGA_PROGSETUP_S.SchDoc
FPGA_TDO
FPGA_TDI
FPGA_TCK
FPGA_TMS
FPGA_DONE
SUSPEND
FPGA_PROGRAM
HOST_HARD_TDO
HOST_HARD_TDI
HOST_HARD_TCK
HOST_HARD_TMS
FLASH_DONE
SUSPEND
FPGA_PROGRAM
ONE_WIRE_DB_PB
ONE_WIRE_DBID
ONE_WIRE_PIO1
ONE_WIRE
U_1WB_DS2406_EPROM
1WB_DS2406_EPROM_S.SchDoc
PIO2
ID
PIO1
ONE_WIRE
U4A
XC3S1400AN-4FG676C
BANK 0
IO_L01N_0
IO_L01P_0
IO_L02N_0
IO_L02P_0/VREF_0
IO_L03N_0
IO_L03P_0
IO_L06N_0
IO_L06P_0
IO_L07N_0
IO_L07P_0
IO_L08N_0
IO_L08P_0
IO_L09N_0
IO_L09P_0
IO_L10N_0
IO_L10P_0
IO_L11N_0
IO_L11P_0
IO_L12N_0
IO_L12P_0
IO_L13N_0
IO_L13P_0
IO_L14N_0
IO_L14P_0/VREF_0
IO_L15N_0
IO_L15P_0
IO_L16N_0
IO_L16P_0
IO_L17N_0
IO_L17P_0
IO_L18N_0
IO_L18P_0
IO_L19N_0
IO_L19P_0
IO_L20N_0/VREF_0
IO_L20P_0
IO_L21N_0
IO_L21P_0
IO_L22N_0
IO_L22P_0
IO_L23N_0
IO_L23P_0
IO_L24N_0
IO_L24P_0
NEXUS_TCK
IO_L25N_0/GCLK5
IO_L25P_0/GCLK4
IO_L26N_0/GCLK7
IO_L26P_0/GCLK6
IO_L27N_0/GCLK9
IO_L27P_0/GCLK8
IO_L28N_0/GCLK11
IO_L28P_0/GCLK10
FPGA_CLK1
U4B
XC3S1400AN-4FG676C
BANK 1
IO_L03N_1/LDC2
IO_L03P_1/HDC
IO_L02N_1/LDC0
IO_L02P_1/LDC1
IO_L01N_1/A11
IO_L01P_1/A0
IO_L00N_1
IO_L04P_1
IO_L05N_1
IO_L05P_1
IO_L06N_1
IO_L06P_1
IO_L07N_1/VREF_1
IO_L07P_1
IO_L08N_1
IO_L08P_1
IO_L09N_1
IO_L09P_1
IO_L10N_1
IO_L10P_1
IO_L11N_1
IO_L11P_1
IO_L12N_1
IO_L12P_1
IO_L13N_1
IO_L13P_1
IO_L14N_1
IO_L14P_1
IO_L15N_1
IO_L15P_1
IO_L16N_1
IO_L16P_1
IO_L17N_1
IO_L17P_1
IO_L18N_1
IO_L18P_1
IO_L19N_1
IO_L19P_1
IO_L20N_1
IO_L20P_1
IO_L21N_1
IO_L21P_1
IO_L22N_1/VREF_1
IO_L22P_1
IO_L23N_1
IO_L23P_1
IO_L24N_1/A3
IO_L24P_1/A2
IO_L25N_1/A5
IO_L25P_1/A4
IO_L26N_1/A7
IO_L26P_1/A6
IO_L27N_1/A9
IO_L27P_1/A8
IO_L28N_1/A10
IO_L28P_1/A12
IO_L29N_1/A13
IO_L29P_1/A14
IO_L41N_1
IO_L41P_1
IO_L42N_1/A17
IO_L42P_1/A16
IO_L43N_1/A19
IO_L43P_1/A18
IO_L46N_1
IO_L46P_1
IO_L47N_1
IO_L47P_1
IO_L49N_1
IO_L49P_1
IO_L50N_1
IO_L50P_1
IO_L51N_1
IO_L51P_1
IO_L53N_1
IO_L53P_1
IO_L54N_1
IO_L54P_1
IO_L56N_1
IO_L56P_1
IO_L57N_1
IO_L57P_1
IO_L58N_1
IO_L58P_1/VREF_1
IO_L59N_1
IO_L59P_1
IO_L60N_1
IO_L60P_1
IO_L61N_1
IO_L61P_1
IO_L62N_1/A21
IO_L62P_1/A20
IO_L63N_1/A23
IO_L63P_1/A22
IO_L64N_1/A25
IO_L64P_1/A24
U4C
XC3S1400AN-4FG676C
BANK 2
IO_L01N_2/M0
IO_L01P_2/M1
IO_L02N_2/CSO_B
IO_L02P_2/M2
IO_L05N_2
IO_L05P_2
IO_L06N_2
IO_L06P_2
IO_L07N_2
IO_L07P_2
IO_L08N_2
IO_L08P_2
IO_L09N_2
IO_L09P_2
IO_L10N_2
IO_L10P_2
IO_L11N_2
IO_L11P_2
IO_L12N_2
IO_L12P_2
IO_L13N_2
IO_L13P_2
IO_L14N_2
IO_L14P_2
IO_L15N_2
IO_L15P_2
IO_L16N_2
IO_L16P_2
IO_L17N_2/VS2
IO_L17P_2/RDWR_B
IO_L18N_2
IO_L18P_2
IO_L19N_2/VS0
IO_L19P_2/VS1
IO_L20N_2
IO_L20P_2
IO_L21N_2/CCLK3
IO_L21P_2/CCLK2
IO_L22N_2/D6
IO_L22P_2/D7
IO_L23N_2
IO_L23P_2
IO_L24N_2/D4
IO_L24P_2/D5
IO_L25N_2/CCLK13
IO_L25P_2/CCLK12
IO_L26N_2/CCLK15
IO_L26P_2/CCLK14
IO_L27N_2/CCLK1
IO_L27P_2/CCLK0
IO_L28N_2/CCLK3
IO_L28P_2/CCLK2
IO_L29N_2
IO_L29P_2
IO_L30N_2/MOSICSI_B
IO_L30P_2
IO_L31N_2
IO_L31P_2
IO_L32N_2/DOUT
IO_L32P_2/AWAKE
IO_L33N_2
IO_L33P_2
IO_L34N_2/D3
IO_L34P_2/INIT_B
IO_L35N_2
IO_L35P_2
IO_L36N_2/D1
IO_L36P_2/D2
IO_L37N_2
IO_L37P_2
IO_L38N_2
IO_L38P_2
IO_L39N_2
IO_L39P_2
IO_L40N_2
IO_L40P_2
IO_L41N_2
IO_L41P_2
IO_L42N_2
IO_L42P_2
IO_L43N_2
IO_L43P_2
IO_L44N_2
IO_L44P_2
IO_L45N_2
IO_L45P_2
IO_L46N_2
IO_L46P_2
IO_L47N_2
IO_L47P_2
IO_L48N_2
IO_L48P_2
IO_L51N_2
IO_L51P_2
IO_L52N_2/CCLK
IO_L52P_2/D0/DIN/MISO
U4D
XC3S1400AN-4FG676C
BANK 3
IO_L01N_3
IO_L01P_3
IO_L02N_3
IO_L02P_3
IO_L03N_3
IO_L03P_3
IO_L04N_3
IO_L04P_3
IO_L07N_3
IO_L07P_3
IO_L08N_3
IO_L08P_3
IO_L09N_3
IO_L09P_3
IO_L10N_3
IO_L10P_3
IO_L11N_3
IO_L11P_3
IO_L12N_3
IO_L12P_3
IO_L13N_3
IO_L13P_3
IO_L14N_3
IO_L14P_3
IO_L15N_3
IO_L15P_3
IO_L16N_3
IO_L16P_3
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IO_L21P_3
IO_L22N_3
IO_L22P_3
IO_L23N_3
IO_L23P_3
IO_L24N_3
IO_L24P_3
IO_L25N_3/VREF_3
IO_L25P_3
IO_L26N_3
IO_L26P_3
IO_L27N_3
IO_L27P_3
IO_L28N_3
IO_L28P_3
IO_L29N_3/VREF_3
IO_L30N_3
IO_L30P_3
IO_L31N_3
IO_L31P_3
IO_L32N_3/HCLK1
IO_L32P_3/HCLK0
IO_L33N_3/IRDY1/LHCLK3
IO_L33P_3/HCLK2
IO_L34N_3/HCLK5
IO_L34P_3/HCLK4
IO_L35N_3/HCLK7
IO_L35P_3/TRDY1/LHCLK6
IO_L36N_3
IO_L36P_3/VREF_3
IO_L37N_3
IO_L37P_3
IO_L38N_3
IO_L38P_3
IO_L39N_3
IO_L39P_3
IO_L40N_3
IO_L40P_3
IO_L41N_3
IO_L41P_3
IO_L42N_3
IO_L42P_3
IO_L43N_3
IO_L43P_3/VREF_3
IO_L44N_3
IO_L44P_3
IO_L45N_3
IO_L45P_3
IO_L47N_3
IO_L47P_3
IO_L48N_3
IO_L48P_3
IO_L49N_3
IO_L49P_3
IO_L51N_3
IO_L51P_3
IO_L52N_3
IO_L52P_3
IO_L53N_3
IO_L53P_3
IO_L56N_3
IO_L56P_3
IO_L57N_3
IO_L57P_3
IO_L58N_3
IO_L58P_3
IO_L59N_3
IO_L59P_3
IO_L60N_3
IO_L60P_3
IO_L61N_3
IO_L61P_3
IO_L62N_3
IO_L62P_3
IO_L63N_3
IO_L63P_3
IO_L64N_3
IO_L64P_3
U4E
XC3S1400AN-4FG676C
IP_0
IP_0/VREF_0
IP_L16N_1
IP_L16P_1
IP_L20N_1/VREF_1
IP_L20P_1
IP_L24N_1/VREF_1
IP_L24P_1
IP_L28N_1
IP_L28P_1/VREF_1
IP_L32N_1
IP_L32P_1
IP_L36N_1
IP_L36P_1/VREF_1
IP_L40N_1
IP_L40P_1
IP_L44N_1
IP_L44P_1/VREF_1
IP_L48N_1
IP_L48P_1
IP_L52N_1/VREF_1
IP_L52P_1
IP_L65N_1
IP_L65P_1/VREF_1
IP_2
IP_2/VREF_2
IP_L04N_3/VREF_3
IP_L04P_3
IP_L08N_3
IP_L08P_3
IP_L12N_3/VREF_3
IP_L12P_3
IP_L16N_3
IP_L16P_3
IP_L20N_3/VREF_3
IP_L20P_3
IP_L24N_3
IP_L24P_3
IP_L28N_3/VREF_3
IP_L28P_3
IP_L34N_3
IP_L34P_3
IP_L62N_3
IP_L62P_3/VREF_3
IP_L66N_3/VREF_3
IP_L66P_3
INTERNAL XC3SxxxAN CONFIGURATION
DISWAP (INT PULLED UP VIA FIXED RESISTOR)
HSWAP LOW= INT PULLUPS OFF
HSWAP LOW= INT PULLUPS ON
XC3S1400AN MODE PIN CONFIGURATIONS
M2 M1 M0 FUNCTION:
0 0 0 PLATFORM FLASH MODE
0 0 1 SPI MODE (MASTER)
0 1 0 BYTE PARALLED INTERFACE
0 1 1 INTERNAL MASTER SPI FLASH
1 0 0 <RESERVED>
1 0 1 JTAG MODE
1 1 0 SLAVE PARALLEL
1 1 1 SLAVE SERIAL
M0 (INT PULL UP VIA HSWAP)
ST ART ADD = 0x0, ADD INCREMENTING
ST ART ADD = 0xFF_FFFF DECREMENTING
M1 (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
M2 (INT PULL UP VIA HSWAP)
MUST BE PULLED LOW DURING CONFIG
XC3S1400AN SPI MODE CONFIGURATIONS
VS2 VS1 VS0 FUNCTION:
0 0 0 <RESERVED>
0 0 1 <RESERVED>
0 1 0 <RESERVED>
0 1 1 <RESERVED>
1 0 0 <RESERVED>
1 0 1 (0x01) STANDARD READ
1 1 0 (0x03) READ ARRAY
1 1 1 (0x0B) SPI FAST READ
VS0 SPI ACCESS SPEED (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
SPI SET TO FAST (0x0B)
VS1 SPI ACCESS SPEED (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
SPI SET TO FAST (0x0B)
VS2 SPI ACCESS SPEED (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
SPI SET TO FAST (0x0B)
PROG_B (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
DONE (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
NOTE:
INTERNAL PULLUP AND PULLDOWN CONFIGURATION RESISTORS ON INPUT ONLY PINS ALLOW CONFIGURATION OF CERTAIN ARM SETTINGS SUCH AS NAND TYPE ETC.
XC3S1400AN DESIGN NOTES:
INTERNAL XC3SxxxAN RESISTANCE VALUES
RPU - PULL UP RESISTOR (VCCO = 3V3) = 10KΩ OHMS
RPD - PULL DOWN RESISTOR (VCCO = 3V3) = 34K5 OHMS
LDC0 (INT PULL UP VIA HSWAP)
HSWAP WILL DISABLE CS OF BPI FLASH
BPI FLASH CONTROL
XC3S1400AN DIR BPI FLASH
LDC0 --> CE#/CS#
LDC1 --> OE#
LDC2 --> BYT E#
HDC --> WE#
D[7..0] --> D[7..0]
A[n..1] --> A[n..1]
A0 --> DQ15A-1
CSI_B <-- PULL LOW
RDWR_B PULL LOW
CCLK (INT PULL UP VIA HSWAP)
DO NOT DRIVE CCLK
ROUTE CCLK WITH SIGNAL INTEGRITY
XC3S1400AN SPI SERIAL INTERFACE
MINIMUM SPI DEVICE SIZE FOR AN XC3S1400AN IS BITS REQUIRED: 4,755,296 - SIZE: 8MBit (M25P80)
CSI_B
MUST BE PULLED LOW DURING CONFIG
(APPLIES TO SPARTAN-3E ONLY - NOT REQUIRED FOR AN)
RDWR_B
MUST BE PULLED LOW DURING CONFIG
(APPLIES TO SPARTAN-3E ONLY - NOT REQUIRED FOR AN)
STATUS_LED
NT6
FPGA_DONE
NOTE:
THESE PINS ARE EXCLUSIVE FROM PIN SWAPPING (GD)
FPGA_PROGRAM
FPGA_TDO
FPGA_INIT
FPGA_DONE
R1
R2
R3
R4
48.7 1%
BOOT FROM INTERNAL FLASH
M2 M1 M0
0 1 1
FPGA_M2
FPGA_M1
FPGA_M0
R39
R37
R38
48.7 1%
GND
3V3
Sheet Title Xilinx XC3S1400AN Host FPGA
Project Title DB4S - XC3S1400AN ARM9 DB
Size: A2
Assy: D-820-00354
RevisionD1
Date: 9/23/2011
Time: 12:00:42 AM
Sheet 2 of 16
File: FPGA_SCH.SchDoc
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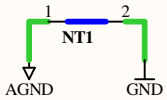
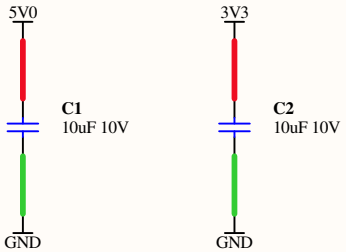
Shared Bypass Caps





U_PSU_MAX1831_1V2
PSU_MAX1831_1V25.SchDoc

Sheet Title	*Power Supply Top Level*		
Project Title	*DB45 - XC3S1400AN ARM9 DB*		
Size: A4	Assy: D-820-0034	Revision: 01	
Date: 9/24/2011	Time: 12:00:42 AM	Sheet 3 of 16	
File: PSU.SCHDOC			

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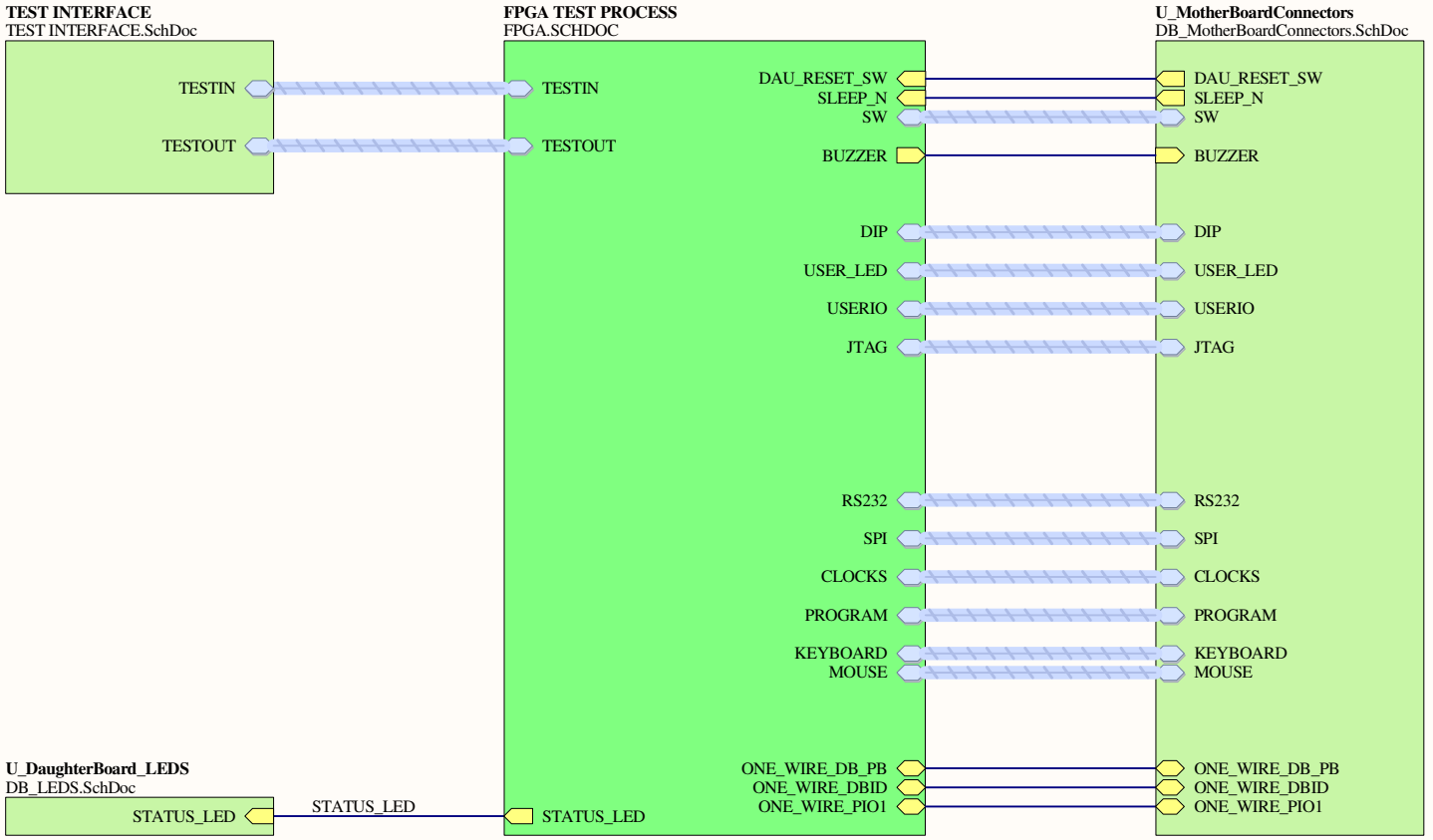

Sheet Title	***Daughter Board Top Level***	
Project Title	***DB45 - XC3S1400AN ARM9 DB***	
Size: A4	Assy: D-820-0034	Revision: 01
Date: 9/24/2011	Time: 12:00:42 AM	Sheet 4 of 16
File: DB_Common.SchDoc		

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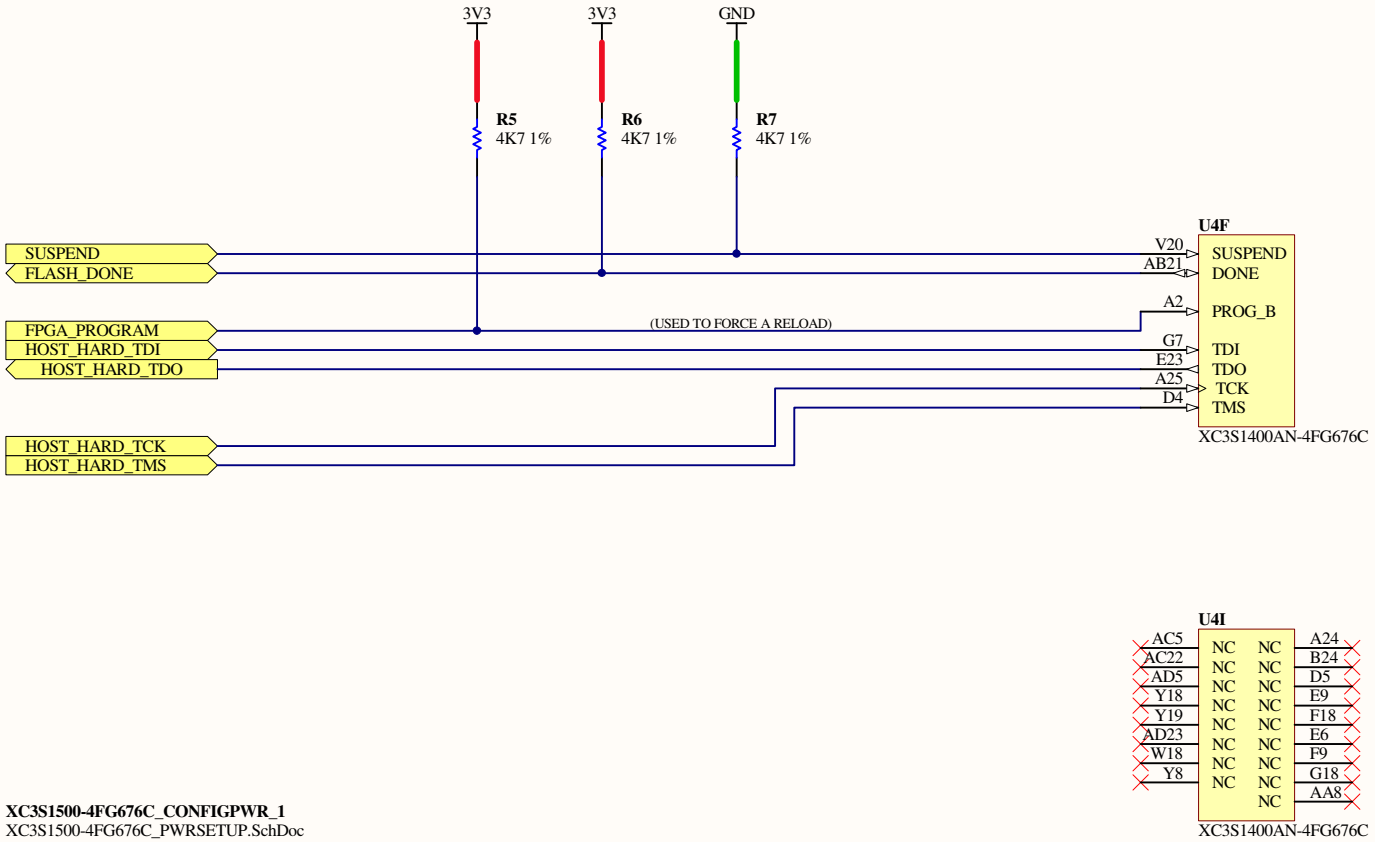

XC3S1500-4FG676C_CONFIGPWR_1
XC3S1500-4FG676C_PWRSETUP.SchDoc

Sheet Title	*XC3S1500-4FG676C Configuration*		
Project Title	*DB45 - XC3S1400AN ARM9 DB*		
Size: A4	Assy: D-820-0034	Revision: 01	
Date: 9/24/2011	Time: 12:00:42 AM	Sheet 5 of 16	
File: FPGA_PRGSETUP.SchDoc			

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1V25

DECOUPLING_CAPS_1V25_1
FPGA_Bypass_1V25.SCHDOC

3V3

DECOUPLING_CAPS_3V3_1
FPGA_Bypass_3V3.SCHDOC

I/O 3.3V

AUX 3.3V

CORE 1.25V

U4H
XC3S1400AN-4FG676C

W24	GND	GND	A1
W19	GND	GND	A6
W14	GND	GND	A11
W8	GND	GND	A16
V3	GND	GND	A21
U17	GND	GND	A26
U13	GND	GND	AA1
U10	GND	GND	AA6
T26	GND	GND	AA11
T21	GND	GND	AA16
T16	GND	GND	AA21
T14	GND	GND	AA26
T12	GND	GND	AD3
T6	GND	GND	AD8
T1	GND	GND	AD13
R15	GND	GND	AD18
R13	GND	GND	AD24
R11	GND	GND	AF1
P24	GND	GND	AF6
P19	GND	GND	AF11
P16	GND	GND	AF16
P12	GND	GND	AF21
N15	GND	GND	AF26
N11	GND	GND	C3
N8	GND	GND	C9
N3	GND	GND	C14
M16	GND	GND	C19
M14	GND	GND	C24
M12	GND	GND	F1
L26	GND	GND	F6
L21	GND	GND	F11
L15	GND	GND	F16
L13	GND	GND	F21
L11	GND	GND	F26
L6	GND	GND	H3
L1	GND	GND	H8
K17	GND	GND	H14
K10	GND	GND	H19
	GND	GND	J24
		GND	

GND GND

3V3 3V3 3V3 3V3

U4G
XC3S1400AN-4FG676C

3V3 1V25

B5	VCCO_0	VCCAUX	AB5
B11	VCCO_0	VCCAUX	AB11
B16	VCCO_0	VCCAUX	AB22
B22	VCCO_0	VCCAUX	E5
E8	VCCO_0	VCCAUX	E16
E13	VCCO_0	VCCAUX	E22
E19	VCCO_0	VCCAUX	J18
H11	VCCO_0	VCCAUX	K13
H16	VCCO_0	VCCAUX	L5
		VCCAUX	N10
AB25	VCCO_1	VCCAUX	P17
E25	VCCO_1	VCCAUX	T22
H22	VCCO_1	VCCAUX	U14
L19	VCCO_1	VCCAUX	V9
L25	VCCO_1		
N22	VCCO_1	VCCINT	K15
T19	VCCO_1	VCCINT	L12
T25	VCCO_1	VCCINT	L14
W22	VCCO_1	VCCINT	L16
		VCCINT	M11
AB8	VCCO_2	VCCINT	M13
AB14	VCCO_2	VCCINT	M15
AB19	VCCO_2	VCCINT	M17
AE5	VCCO_2	VCCINT	N12
AE11	VCCO_2	VCCINT	N13
AE16	VCCO_2	VCCINT	N14
AE22	VCCO_2	VCCINT	N16
W11	VCCO_2	VCCINT	P11
W16	VCCO_2	VCCINT	P13
	VCCO_2	VCCINT	P14
		VCCINT	P15
AB2	VCCO_3	VCCINT	R12
E2	VCCO_3	VCCINT	R14
H5	VCCO_3	VCCINT	R16
L2	VCCO_3	VCCINT	T11
L8	VCCO_3	VCCINT	T13
P5	VCCO_3	VCCINT	T15
T2	VCCO_3	VCCINT	U12
T8	VCCO_3	VCCINT	
W5	VCCO_3		
	VCCO_3		

Sheet Title	*XC3S1500-4FG676C POWER*		
Project Title	*DB45 - XC3S1400AN ARM9 DB*		
Size: A4	Assy: D-820-0034	Revision: 01	
Date: 9/24/2011	Time: 12:00:42 AM	Sheet 6 of 16	
File: XC3S1500-4FG676C_PWRSETUP.SchDoc			

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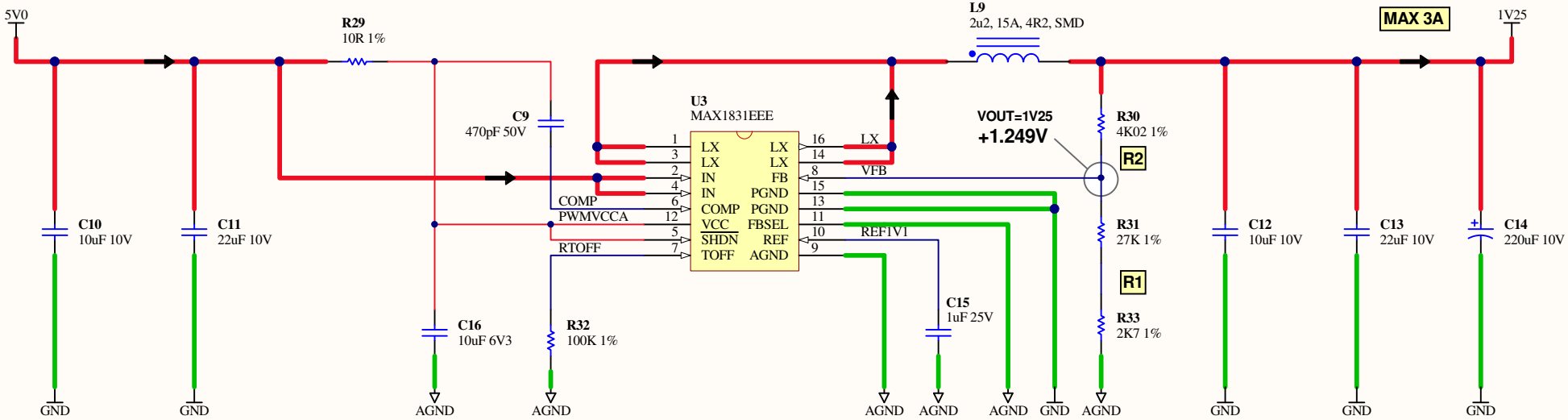

R1 = 30K

VREF = 1.10V

R2 = R1 ($\frac{VOUT}{VREF}$ -1)

R2 = 30000 ($\frac{1V25}{1V10}$-1)

R2 = 30000 (1V1363-1)

R2 = 30000 x 0V1363

R2 = 30000 x 0V1363

R2 = 4K089

Sheet Title: *PSU1V25*		
Project Title: *DB45 - XC3S1400AN ARM9 DB*		
Size: A4	Assy: D-820-0034	Revision: 01
Date: 9/24/2011 Time: 12:00:42 AM	Sheet 7 of 16	
File: PSU_MAX1831_1V25.SchDoc		

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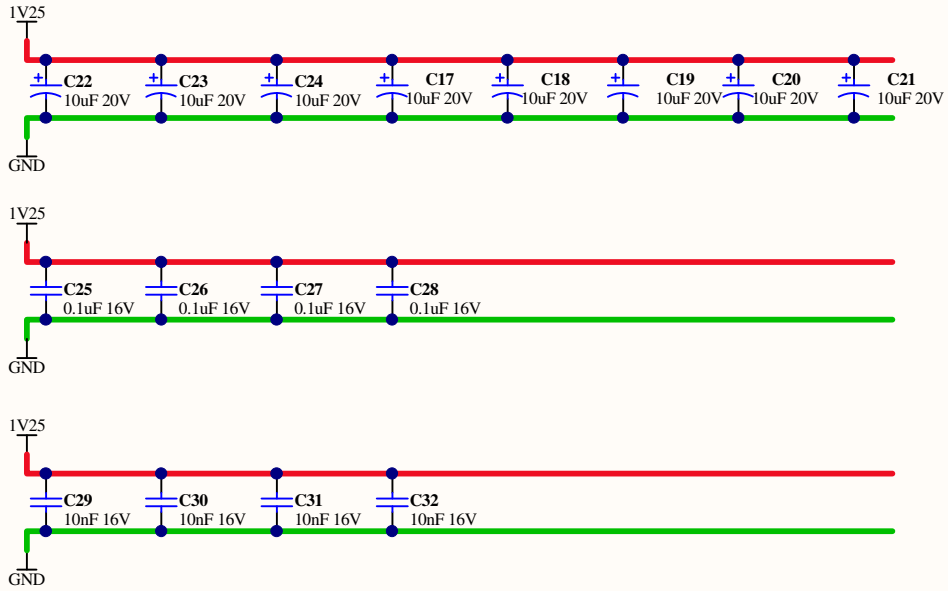

Sheet Title	*FPGA Bypass 1V2*		
Project Title	*DB45 - XC3S1400AN ARM9 DB*		
Size: A4	Assy: D-820-0034	Revision: 01	
Date: 9/24/2011	Time: 12:00:42 AM	Sheet 8 of 16	
File: FPGA_Bypass_1V25.SCHDOC			

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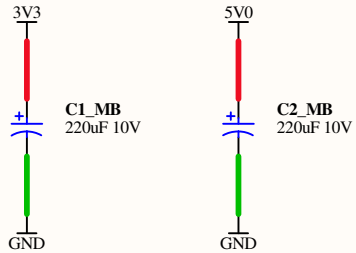

These decoupling capacitors are intended to assist the voltage rails on the PCB - where the decoupling capacitors for the FPGA are not close.

Sheet Title	***Board Bypass Capacitors***		
Project Title	***DB45 - XC3S1400AN ARM9 DB***		
Size: A4	Assy: D-820-0034	Revision: 01	
Date: 9/24/2011	Time: 12:00:42 AM	Sheet 9 of 16	
File: DB_Bypass.SchDoc			

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MH1
MOUNTING HOLE 3MM

MH2
MOUNTING HOLE 3MM

MH3
MOUNTING HOLE 3MM

Altium Logo Top1

Altium Logo Bot1

Sheet Title	***Mounts, Logo & Label***		
Project Title	***DB45 - XC3S1400AN ARM9 DB***		
Size: A4	Assy: D-820-0034	Revision: 01	
Date: 9/24/2011	Time: 12:00:42 AM	Sheet 10 of 16	
File: DB_MOUNTS.SchDoc			

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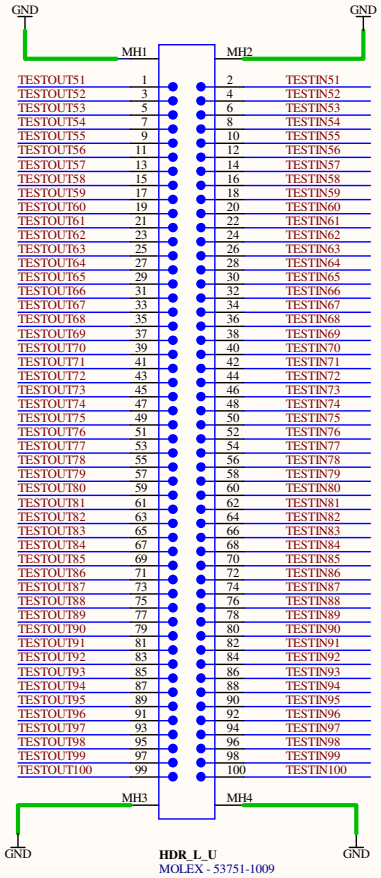

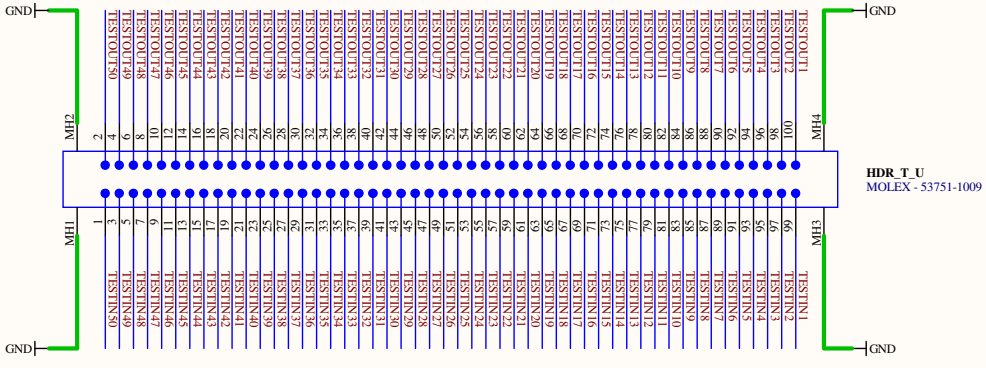

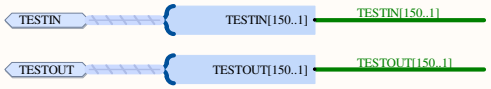

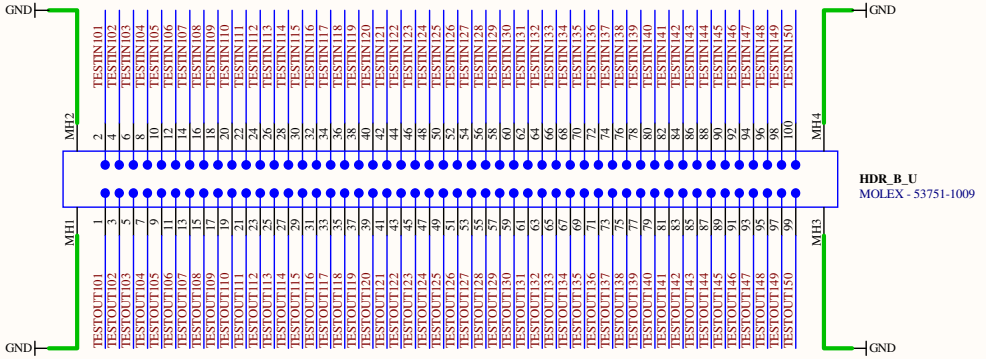

Sheet Title	*Test Interface*		
Project Title	*DB45 - XC3S1400AN ARM9 DB*		
Size: A3	Assy: D-820-0034	Revision: 01	
Date: 9/24/2011	Time: 12:00:42 AM	Sheet 11 of 16	
File: Test Interface.SchDoc			

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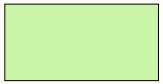
U_MOUNTS
DB_MOUNTS.SchDoc



PCB1
TB11 Blank PCB
Printed Circuit Board (Bare)

Sheet Title	*TB11_Hardware_Kit*		
Project Title	*DB45 - XC3S1400AN ARM9 DB*		
Size: A4	Assy: D-820-0034	Revision: 01	
Date: 9/24/2011	Time: 12:00:42 AM	Sheet 12 of 16	
File: TB11_Hardware_Kit.SchDoc			

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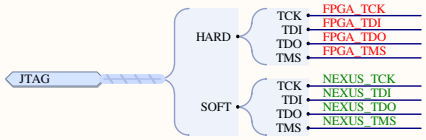
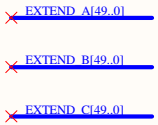
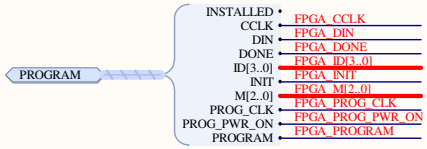
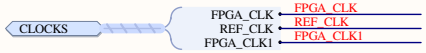
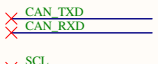
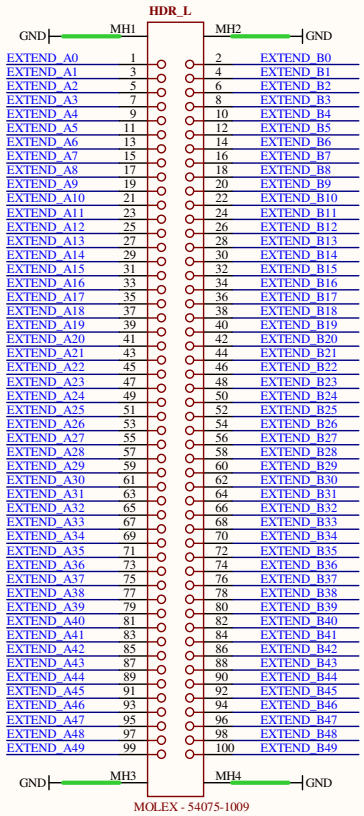


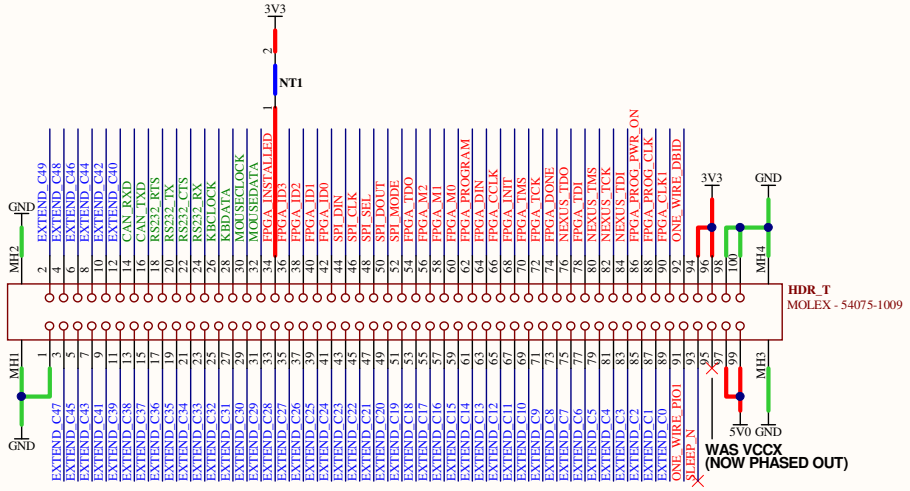






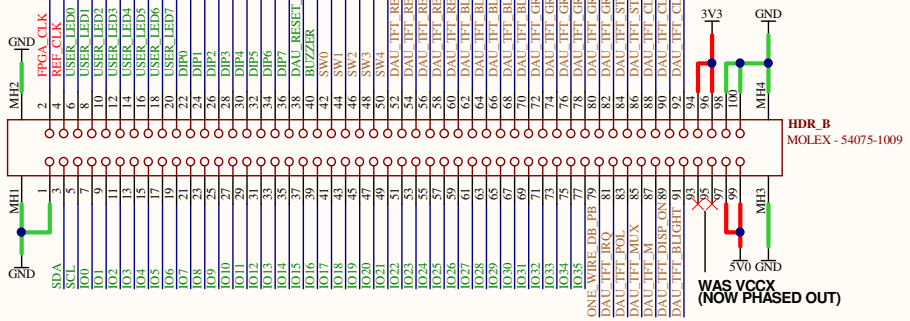






Note that the signal ONE_WIRE_DBID was previously called FPGA_CLK2.

This signal was included in NB1 design, but never used. Hence it has now been reallocated.



Red Connections are locked for NB1 compatibility. They are hardwired on the NB1 and therefore can NOT be changed.

Green connections are I/O pins connected to NB1 compatible PCB resources on the mother board. These can be changed.

Blue connections are connected to the New NB2 compatible resources on the motherboard. These can be changed.

Sheet Title	NB2 to Daughter Board Connectors		
Project Title	DB45 - XC3S1400AN ARM9 DB		
Size: A3	Assy: D-820-0034	Revision: 01	
Date: 9/24/2011	Time: 12:00:42 AM	Sheet 13 of 16	
File: DB_MotherBoardConnectors.SchDoc			

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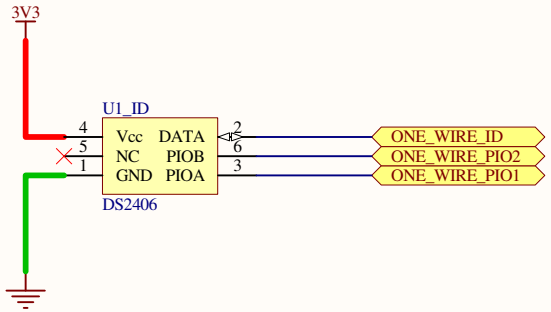

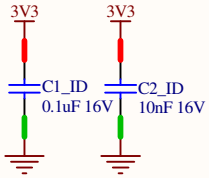

Sheet Title	***1-Wire Bus ID***		
Project Title	***DB45 - XC3S1400AN ARM9 DB***		
Size: A4	Assy: D-820-0034	Revision: 01	
Date: 9/24/2011	Time: 12:00:42 AM	Sheet 14 of 20	
File: 1WB_DS2406_EPROM.SchDoc			

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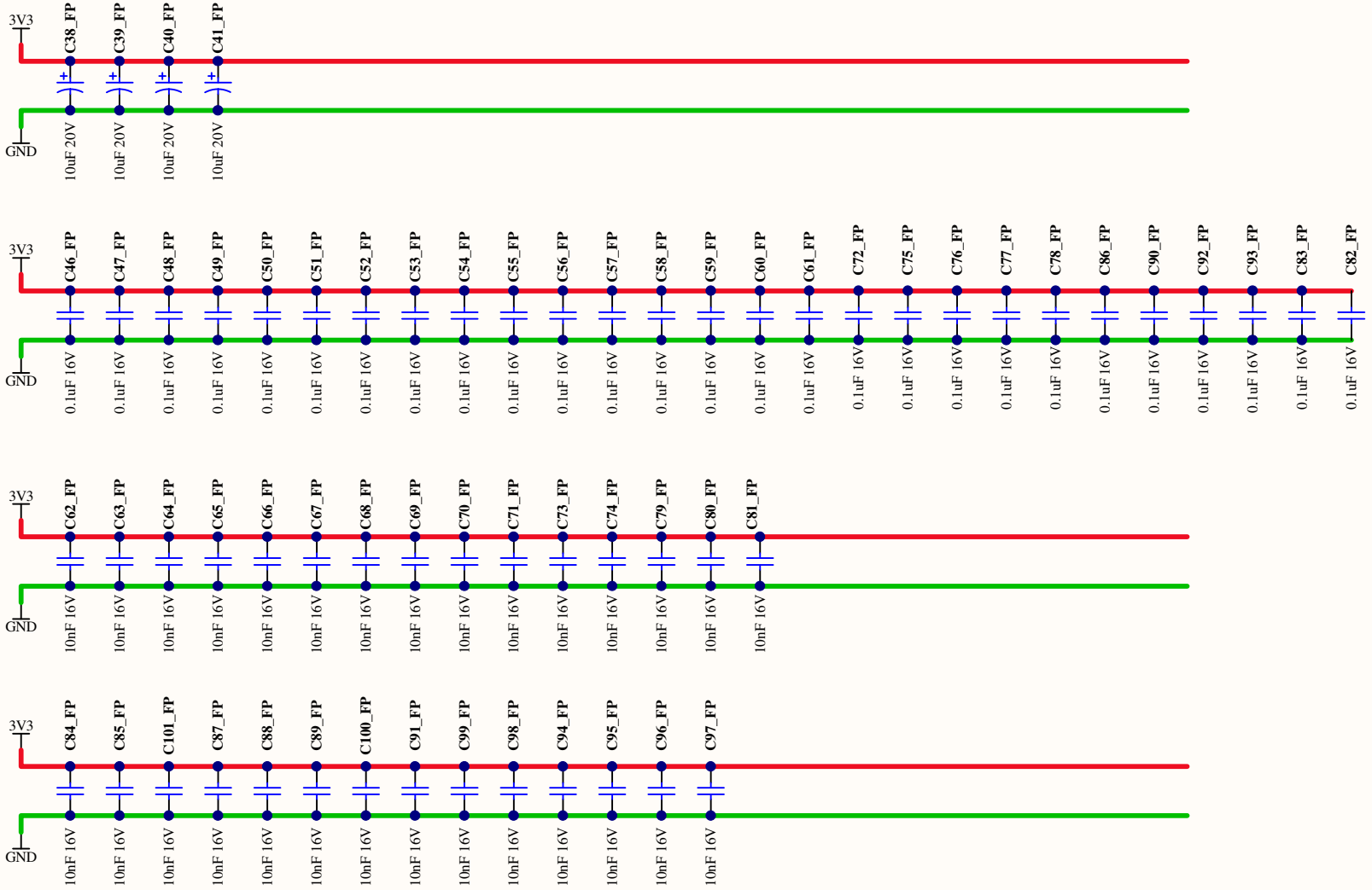

The FPGA bypass capacitors are physically grouped as 10nF and 100nF pairs on all major accessible power pins on the FPGA.

Sheet Title	*FPGA Bypass 3V3*		
Project Title	*DB45 - XC3S1400AN ARM9 DB*		
Size: A4	Assy: D-820-0034	Revision: 01	
Date: 9/24/2011	Time: 12:00:42 AM	Sheet 15 of 16	
File: FPGA_Bypass_3V3.SCHDOC			

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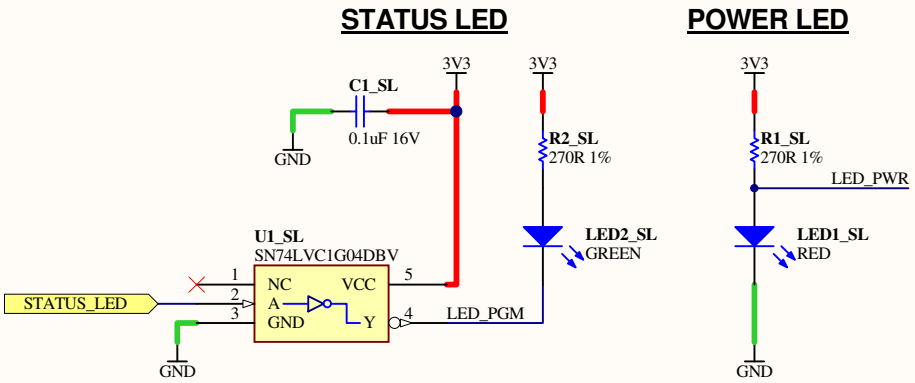

Sheet Title	*Daughter Board LEDs*		
Project Title	*DB45 - XC3S1400AN ARM9 DB*		
Size: A4	Assy: D-820-0034	Revision: 01	
Date: 9/24/2011	Time: 12:00:43 AM	Sheet 16 of 16	
File: DB_LEDS.SchDoc			

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